ISL6206

High Voltage Synchronous Rectified Buck MOSFET Driver

FN9071
Rev.1.00
May 2002

The ISL6206 is a high voltage, high frequency, dual MOSFET driver specifically designed to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter topology in mobile computing applications. This driver combined with an Intersil Multi-Phase Buck PWM controller forms a complete single-stage core-voltage regulator solution for advanced mobile microprocessors.

The ISL6206 features a three-state PWM input that, working together with any Intersil multiphase PWM controllers, will prevent a negative transient on the output voltage when the output is being shut down. This feature eliminates the Schottky diode that is usually seen in a microprocessor power system for protecting the microprocessor from reversed-output-voltage damage.

The output drivers in the ISL6206 has the capacity to efficiently switch power MOSFETs at frequencies up to 2MHz. Each driver is capable of driving a 3000pF load with a 15ns propagation delay and 20ns transition time. This product implements bootstrapping on the upper gate, reducing implementation complexity and allowing the use of higher performance, cost effective, N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ISL6206CB	-10 to 85	8 Ld SOIC	M8.15
ISL6206CB-T	8 Ld SOIC Tape and Reel		

Features

- Drives Two N-Channel MOSFETs
- Adaptive Shoot-Through Protection
- 30V Operation Voltage
- Supports High Switching Frequency
  - Fast Output Rise Time
  - Propagation Delay 15ns
- Three-state Input for Output Stage Shutdown
- Internal Bootstrap Schottky Diode

Applications

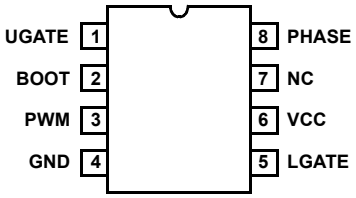
- Core Voltage Supplies for Intel and AMD® Mobile Microprocessors
- High Frequency Low Profile DC-DC Converters
- High Current Low Output Voltage DC-DC Converters
- High Input Voltage DC-DC Converters

Related Literature

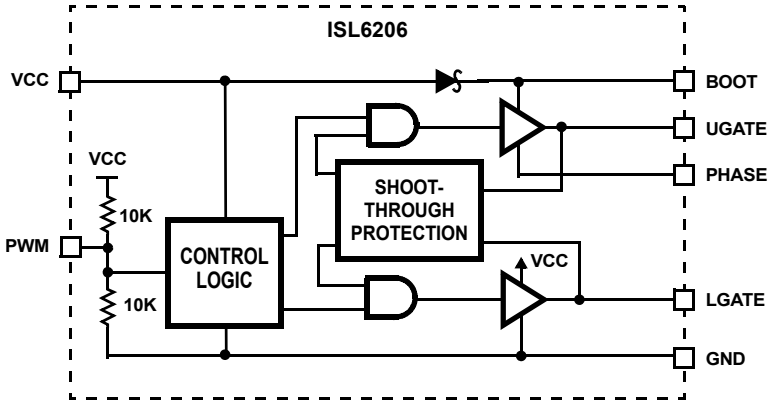
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Pinout

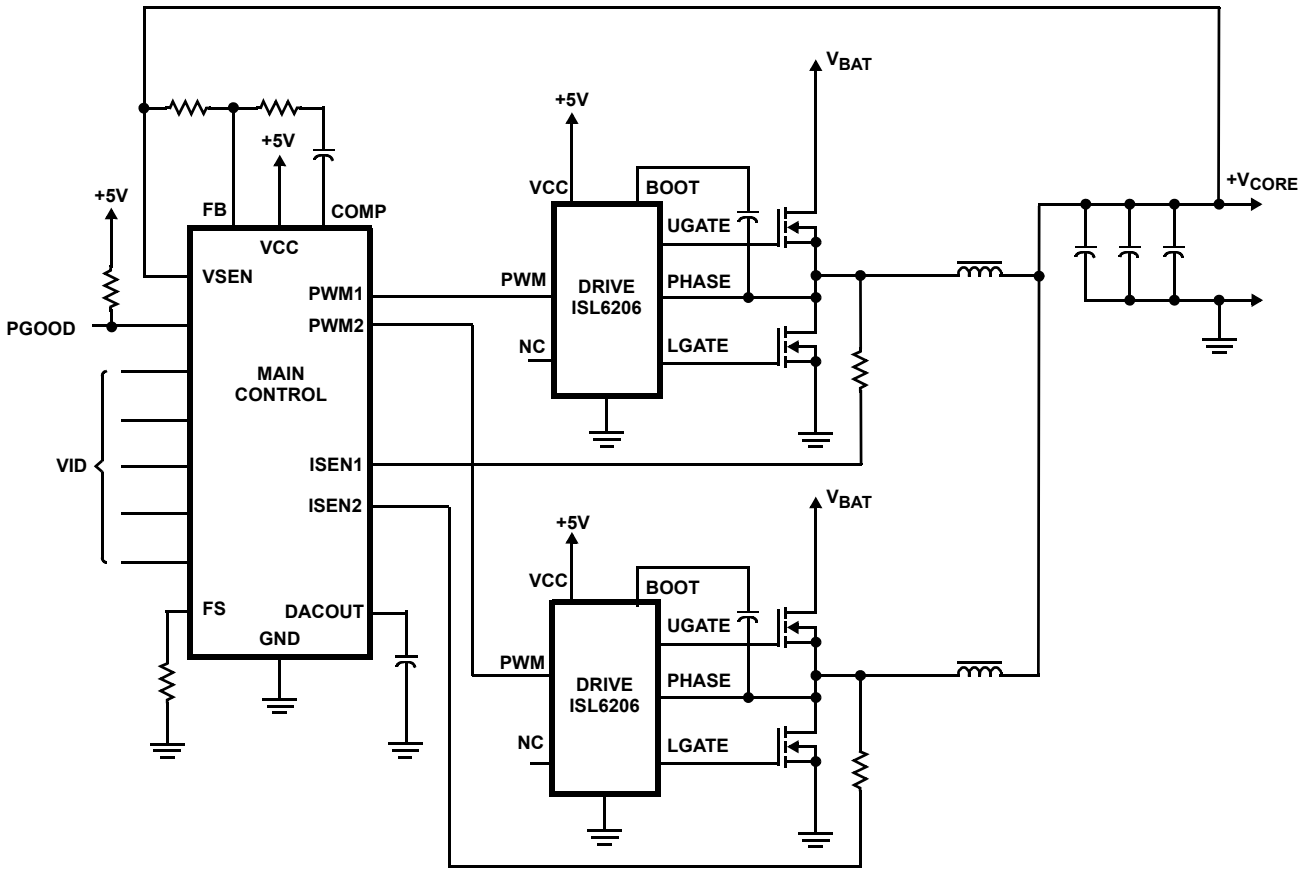
ISL6206CB (SOIC)
TOP VIEW



Block Diagram



Typical Application - Two Phase Converter Using ISL6206 Gate Drivers



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 7V
BOOT Voltage (V_{BOOT}) . . . . . -0.3V to 36V
Phase Voltage (V_{PHASE}) (Note 1) . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
Input Voltage (V_{PWM}) . . . . . -0.3V to VCC + 0.3V
UGATE . . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
LGATE . . . . . -0.3V to VCC + 0.3V
Ambient Temperature Range . . . . . -40°C to 125°C

Recommended Operating Conditions

Ambient Temperature Range . . . . . -10°C to 85°C
Maximum Operating Junction Temperature . . . . . 125°C
Supply Voltage, VCC . . . . . 5V ±10%

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
SOIC Package (Note 2)	110

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The Phase Voltage is capable of withstanding -7V when the BOOT pin is shorted to GND.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	PWM pin floating, V_{VCC} = 5V	-	30	-	µA
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 5V	-	250	-	µA
		V_{PWM} = 0V	-	-250	-	µA
PWM three-state Rising Threshold		V_{VCC} = 5V	-	-	1.7	V
PWM three-state Falling Threshold		V_{VCC} = 5V	3.3	-	-	V
three-state Shutdown Holdoff Time		V_{VCC} = 5V, Temperature = 25° C	-	300	-	ns
SWITCHING TIME						
UGATE Rise Time	t_{RUGATE}	V_{VCC} = 5V, 3nF Load	-	20	-	ns
LGATE Rise Time	t_{RLGATE}	V_{VCC} = 5V, 3nF Load	-	20	-	ns
UGATE Fall Time	t_{FUGATE}	V_{VCC} = 5V, 3nF Load	-	15	-	ns
LGATE Fall Time	t_{FLGATE}	V_{VCC} = 5V, 3nF Load	-	15	-	ns
UGATE Turn-Off Propagation Delay	$t_{PDLUGATE}$	V_{VCC} = 5V, 3nF Load	-	15	-	ns
LGATE Turn-Off Propagation Delay	$t_{PDLLGATE}$	V_{VCC} = 5V, 3nF Load	-	15	-	ns
OUTPUT						
Upper Drive Source Resistance	R_{UGATE}	500mA Source Current	-	3.1	5.0	Ω
Upper Driver Source Current (Note 3)	I_{UGATE}	$V_{UGATE-PHASE}$ = 2.5V	-	700	-	mA
Upper Drive Sink Resistance	R_{UGATE}	500mA Sink Current	-	1.5	2.6	Ω
Upper Driver Sink Current (Note 3)	I_{UGATE}	$V_{UGATE-PHASE}$ = 2.5V	-	1.1	-	A
Lower Drive Source Resistance	R_{LGATE}	500mA Source Current	-	3.1	5.0	Ω
Lower Driver Source Current (Note 3)	I_{LGATE}	V_{LGATE} = 2.5V	-	700	-	mA
Lower Drive Sink Resistance	R_{LGATE}	500mA Sink Current	-	1.5	2.6	Ω
Lower Driver Sink Current (Note 3)	I_{LGATE}	V_{LGATE} = 2.5V	-	1.1	-	A

NOTE:

3. Guaranteed by design, not tested.

Functional Pin Description

UGATE (Pin 1)

Upper gate drive output. Connect to the gate of the high-side N-Channel power MOSFET.

BOOT (Pin 2)

Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Bootstrap Diode and Capacitor section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

PWM (Pin 3)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of any Intersil multiphase controllers.

GND (Pin 4)

Ground pin. All signals are referenced to this node.

LGATE (Pin 5)

Lower gate drive output. Connect to the gate of the low-side N-Channel power MOSFET.

VCC (Pin 6)

Connect this pin to a +5V bias supply. Place a high quality bypass capacitor from this pin to GND.

NC (Pin 7)

No connection. Leave this pin floating.

PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

Description

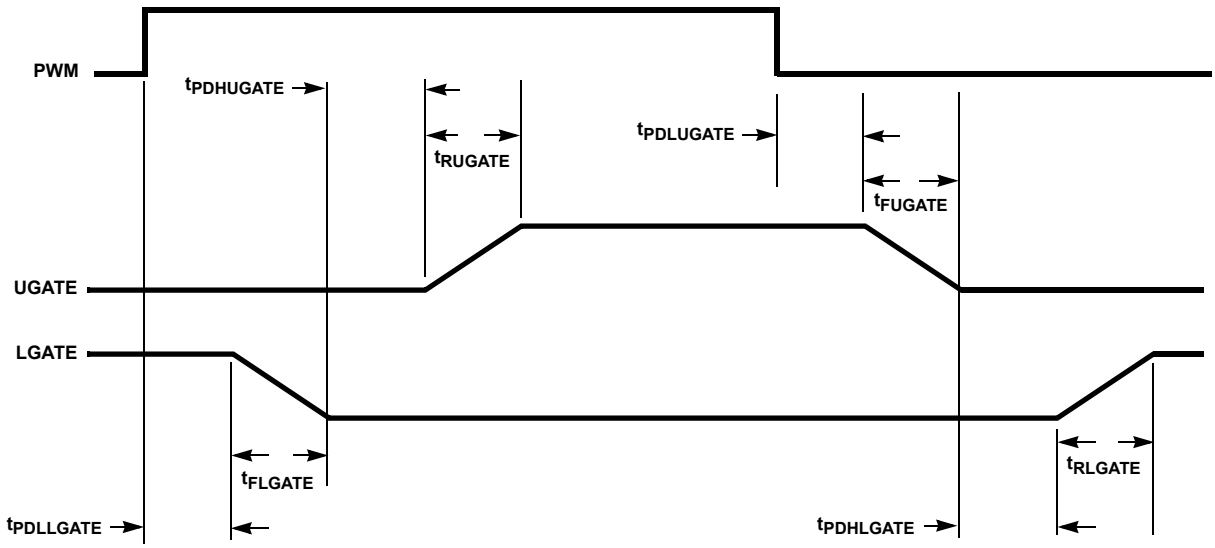
Operation

The ISL6206 dual MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [$t_{PDLLGATE}$], the lower gate begins to fall. Typical fall times [t_{FLGATE}] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$t_{PDHUGATE}$] based on how quickly the LGATE voltage drops below 1V. This prevents both the lower and upper MOSFETs from conducting simultaneously or shoot-through. Once this delay period is complete the upper gate drive begins to rise [t_{RUGATE}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$t_{PDLUGATE}$] is encountered before the upper gate begins to fall [t_{FUGATE}]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $t_{PDHLGATE}$. The upper MOSFET gate voltage is monitored and the lower gate is allowed to rise after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [t_{RLGATE}], turning on the lower MOSFET.

Timing Diagram



Three-state PWM Input

A unique feature of the ISL6206 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled.

Adaptive Shoot-Through Protection

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the gate driver has turned off one MOSFET before the gate voltage of the other MOSFET is allowed to rise.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the upper MOSFET gate voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

Bootstrap Diode and Capacitor

This driver features an internal Schottky bootstrap diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

The bootstrap capacitor must have a maximum voltage rating above the maximum battery voltage plus 5V. The bootstrap capacitor can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}}$$

where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge, Q_{GATE}, of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.22µF. A good quality ceramic capacitor is recommended.

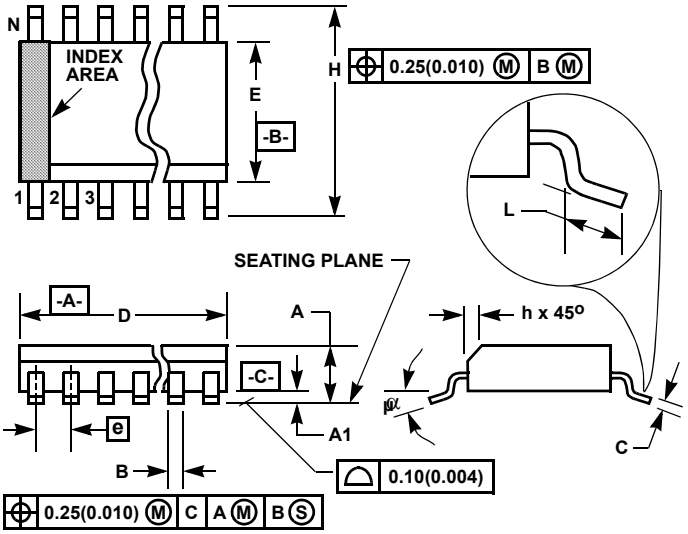
Power Dissipation

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO-8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as:

$$P = f_{sw}(1.5V_U Q_U + V_L Q_L) + I_{DDQ} V_{CC}$$

where f_{sw} is the switching frequency of the PWM signal. V_U and V_L represent the upper and lower gate rail voltage. Q_U and Q_L is the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The I_{DDQ} V_{CC} product is the quiescent power of the driver and is negligible.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93