RAGE MOBILITY M6/D6/P6

Graphics Subsystem Design Guide

PRELIMINARY

Technical Reference Manual

P/N: DSG-216M6-00-03

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1 Introduction

1.1 About This Manual

Use this manual along with the RAGE MOBILITY M6 Reference Design Schematics to help you design a graphics subsystem based on ATI's RAGE MOBILITY M6 graphics controller. This manual is intended for experienced design engineers.

1.2 Scope

This manual should be used with the RAGE MOBILITY M6 Reference Design Schematics. Use this manual to help you integrate the RAGE MOBILITY M6 graphics controller into a motherboard-based graphics subsystem or into an add-in graphics adapter. The content of this manual focuses on general design considerations for:

- Component layout.
- Signal routing and termination.
- Noise filtering.
- Power and grounding requirements.
- Configuration and feature options.
- Exceptions and deviations (and their potential effects).

To ensure the integrity and robustness of your RAGE MOBILITY M6-based graphics subsystem, adhere to the recommendations of this manual.

1.3 Supported Controllers

This manual supports the following types of RAGE MOBILITY controllers:

Table 1: Supported RAGE MOBILITY Controllers

RAGE MOBILITY M6 Graphics Controller Model	BGA Package	Reference Schematic P/N	Graphics Controller Specification P/N
RAGE MOBILITY P6	484-pin	105-REF88-00C	CHS-216M6-00-01
RAGE MOBILITY M6	484-pin	105-REF87-00C	CHS-216M6-00-01
RAGE MOBILITY D6	484-pin	105-REF87-00C	CHS-216M6-00-01

2 Graphics Subsystem Overview

This section is an overview of a RAGE MOBILITY M6-based graphics subsystem. Some aspects of this section will overlap with other sections. The remaining sections provide additional details regarding each specific interface. A graphics subsystem can be viewed as a collection of interfaces (functional blocks) to a graphics controller. The supported functions will depend on the features supported by a specific graphics controller.

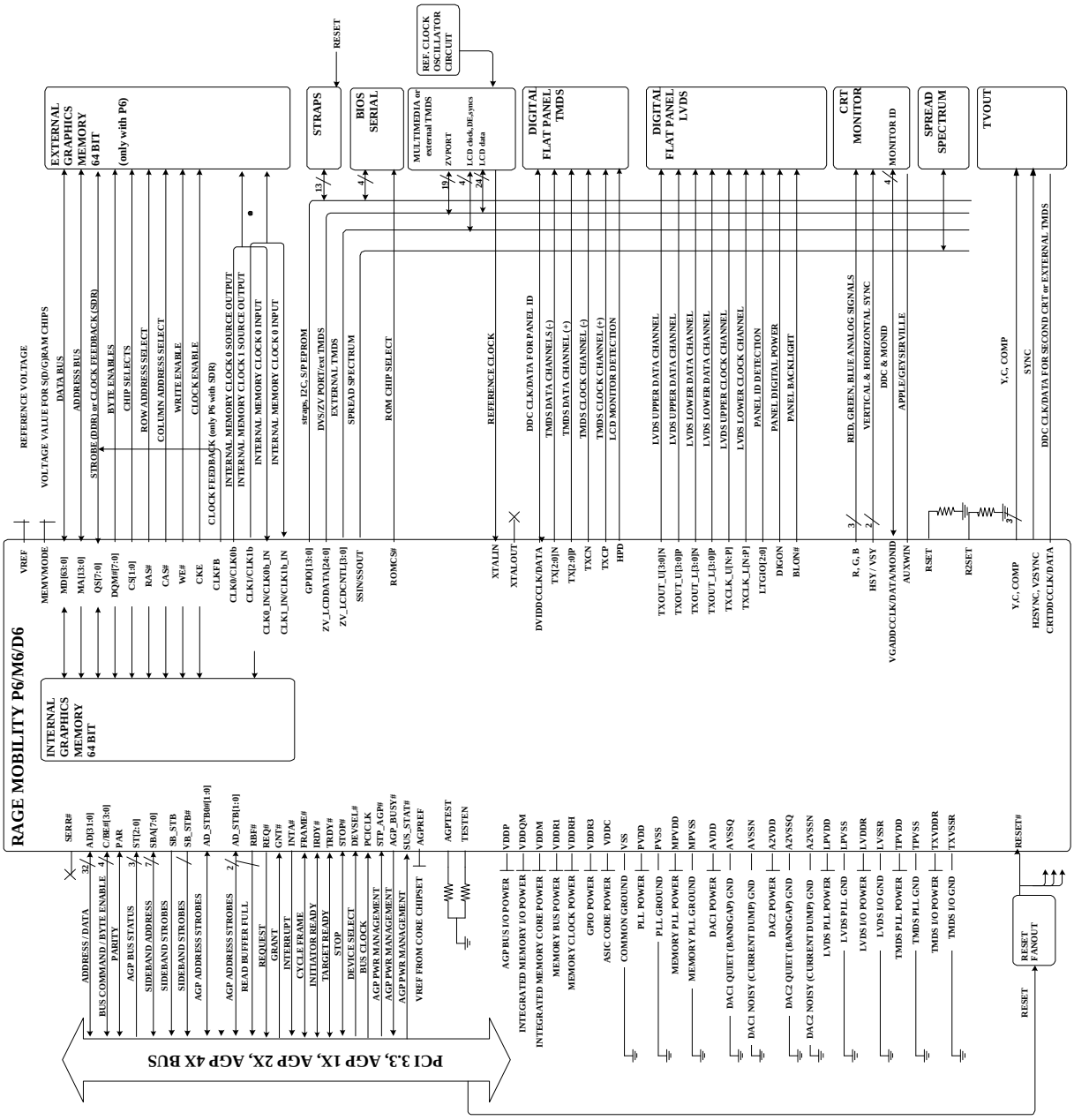


Figure 1: RAGE MOBILITY M6 Graphics Subsystem

2.1 Considerations for the Layout of the Subsystem

High-speed digital signals can generate large ground-current spikes that appear on the circuit's noise floor. Use the following guidelines so that the digital signals will be properly bypassed, kept away from sensitive circuit areas, and analog supplies.

- Keep digital signals away from analog signals.
- Keep digital components and wires as far away from analog sections as possible.
- Avoid routing digital signals through analog sections.
- Keep sensitive nets short by placing analog components close to the chip, and short wires over their respective planes. Keep a careful watch on RSET, R2SET, XTALIN, and XTALOUT signals.
- Place bypass capacitors as close as possible to each power pin.
- For 4-layer PCBs, position the ground plane closest to the component side and position the power plane closest to the solder side.
- For add-in board designs, join all ground nets at one location as close as possible to the card edge connector.
- Use a low impedance ground (i.e., a continuous ground plane).
- Provide separate filtered power supplies for analog functions.
- To reduce EMI and comply with FCC requirements, install capacitors and ferrite beads on the RGB signals.
- When routing the AGP interface signals, closely follow the AGP specification.
- Avoid using sockets.
- To reduce path impedance, use multi-via pads for power and ground pad connections.
- Keep trace lengths as short as possible.
- To minimize cross talk, sandwich all high-frequency signal traces between ground traces or planes.
- For traces that carry high-frequency signals, avoid using sharp corners or bends.

2.2 Subsystem Grounding

Uniform ground planes is the preferred grounding topology because macros are given a solid ground reference.

Uniform grounding minimizes the ground bounce due to switching currents.

All macros attached to common analog grounds and supplies should have wide, short, and low impedance paths to the ground plane. On the graphics controller, supplies and grounds are logically separated into pairs, such as PVDD and PVSS.

2.3 Power Supply Decoupling

For a detailed discussion about power and ground considerations, refer to Chapter 3.

The following is a brief discussion about power supply decoupling.

The core-power supply loop is susceptible to EMI (i.e., electromagnetic interference). This loop includes the power supply, the VDDC and VSS ground planes, as well as the controller's power pins. To reduce EMI, minimize the size of this loop to contain the noise in a smaller area.

Use the following design tips:

- Use bypass capacitors (sometimes in multiples). Place the capacitors as close as possible to the controller's VDDC pin and VSS ground plane.
- Install bypass capacitors on all power pins.
- To filter out high frequency noise on the PLL supply, use multiple bypass capacitors.
- Use electrolytic capacitors for decoupling purposes.

2.4 Optionally Unused Pins

Table 2: Optionally Unused Pins

Interface	Pin Name	I/O	Functions	Action if not Implemented (PD/ PU/ NC)	Comment
Host PCI/AGP	RSTb	I	Active Low PCI Reset		Must stay connected
	PCICLK	I	Bus Clock,		Must stay connected
	AD(31:0)	I/O	Address/Data (31:0)		Must stay connected
	C/BEb(3:0)	I/O	Bus Command/ Byte Enable(3:0)		Must stay connected
	FRAMEb	I/O	Cycle Frame		Must stay connected
	IRDYb	I/O	Initiator (bus master) ready		Must stay connected
	TRDYb	I/O	Target device ready		Must stay connected
	DEVSELb	I/O	Device select		Must stay connected
	STOPb	I/O	Target transaction termination request		Must stay connected
	PAR	O	Parity bit for AD(31:0) and C/BEb(3:0)		Must stay connected
	INTAb	O	Interrupt request line		Must stay connected
	REQb	I/O	PCI Bus Master Request signal to arbiter		Must stay connected
	GNTb	I	PCI Bus Master Grant signal from arbiter		Must stay connected
	ST(2:0)	I	AGP Status bus		Must stay connected
	SBA7/IDSEL	I/O	AGP Sideband Address port bit 7 **or** PCI Initialization device select (in PCI mode)		Must stay connected
	SBA(6:0)	O	Sideband Address port for AGP1X/2X support		Must stay connected
	RBFb	O	AGP Read buffer full		Must stay connected
	AD_STB(1:0)	I/O	AGP-133 Address strobe		Must stay connected
	SB_STB	I/O	Sideband Strobe for AGP1X/2X support		Must stay connected
	AD_STBb(1:0)	I/O	AGP-133 Address strobe differential complement		Must stay connected
	SB_STBb	I/O	Sideband Strobe differential complement		Must stay connected

	AGPTEST	I	External fixed reference	**NC**	**AGP4X/2X(1.5V)**: the compensator requires an external fixed reference tυ compare the strength of the chip against. This fixed reference is a resistor to ground, connected to AGPTEST. The compensator will drive the resistor with an output buffer in the AGPTEST pad, and measure the voltage. This voltage is an indication of the strength of the output driver. The compensator will adjust it accordingly. Resistor value should be 45 ohm +/-1% **PCI/AGP2X(3.3V)**: Unused. Leave this pin unconnected
	AGPREF	I	Reference Voltage for differential receivers	**NC**	**AGP4X/2X(1.5V):** this voltage is set to VDDP/2. All the differential receivers have an internal VREF available. The use of internal or external VREF is determined by whether VDDP=3.3V or VDDP=1.5V, respectively. **PCI/AGP2X(3.3V)**: Unused. Leave this pin unconnected
	SERRb	O	**PCI :** System error signal to the PCI Bus	**NC**	This is intended to be used for debug only. Full SERR support such as register support in configuration space, and reception of external SERR conditions is not intended. **Do not connect this signal on production boards.** This pin is also reserved for WBFb if it is ever required by future designs.
Bus Power Man.	STP_AGPb	I	Power management signal for AGP bus.	**PU**	**AGP :** graphics controller monitors this signal to find out when the CPU is about to enter S0/C3, S1, S2, S3 states. The southbridge generates this signal.
	AGP_BUSYb	O	Power management signal for AGP bus.	**PU**	**AGP :** When asserted (active low), it indicates that the AGP device is currently busy and the AGP clock should not be stopped (meaning that the Host clock can't be stopped). The operating system should then transition into the C2 state instead of the C3 state. When de-asserted (active high), it indicates that the AGP device is not running any cycles and the AGP clock could be stopped.

	SUS_STATb	I	Provides indication when AGP clock is about to stop. Should be connected to ***SUS_STAT#*** signal from the chipset.	**PU**	Pull up to the 3.3V if not used
Memory SDRAM / SGRAM	DQ(63:0)	I/O	Memory Data Bus Supports SSTL2 and SSTL3 (DDR), and LVTTL (SDR)	**NC**	Leave open if not used. (have internal pull ups)
	DQMb(7:0)	O	Byte enables Memory data byte enables for write cycles	**NC**	Leave open if not used. (have internal pull ups)
	ADDR(13:0)	O	Memory Address Bus Provide multiplexed row and column addresses to the S(D/G)RAMs AA(13) is always BA(0). AA(12) is BA(1) for 4 bank S(D/G)RAMs and A(12) for 2 bank S(D/G)RAMs.	**NC**	Leave open if not used. (have internal pull downs) Straps still applicable.
	CSb(1:0)	O	Chip selects and upper row addresses to the S(D/G)RAMs	**NC**	Leave open if not used. (have internal pull ups)
	QS(7:0)	I/O	DDR data strobes, these strobes are used to latch data into the chip and the DDR S(D/G)RAMs.	**NC**	Leave open if not used. (have internal pull downs)
	RASb	O	Row Address Strobe	**NC**	Leave open if not used. (has internal pull up)
	CASb	O	Column Address Strobe	**NC**	Leave open if not used. (has internal pull up).
	WEb	O	Write enable	**NC**	Leave open if not used. (has internal pull up)
	CKE	O	Clock enable control	**NC**	Leave open if not used. (has internal
	CLK0	I/O	Memory clock 0		Must stay connected
	CLK0b	I/O	Memory clock 0 bar , required for external feedback for DLLs	**NC**	If DDR is used must stay connected. If DDR is not used leave open (has internal pull up)
	CLK1	I/O	Memory clock 1	**NC**	If two DDR memory chips are used this is the clock for the second chip and must stay connected. If DDR is not used leave open. (has internal pull down)
	CLK1b	I/O	Memory clock 1 bar, required for external feedback for DLLs	**NC**	If two DDR memory chips are used this is the negative clock for the second chip and must stay connected. If DDR is not used leave open. (has internal pull up)
	CLKFB	O	Feedback clock	**NC**	Used only for SDR memory. Leave open if not used. (has internal pull down)

	CLK0_IN	I	Internal SDRAM memory clock 0 (lower 32-bits)		Must stay connected
	CLK0b_IN	I	Internal SDRAM memory clock 0 bar (lower 32-bits)	**NC**	If DDR is used must stay connected. If DDR is not used leave open (has internal pull up)
	CLK1_IN	I	Internal SDRAM memory clock 1 (upper 32-bits)	**NC**	If two DDR memory chips are used this is the clock for the second chip and must stay connected. If DDR is not used leave open. (has internal pull down)
	CLK1b_IN	I	Internal SDRAM memory clock 1 bar (upper 32-bits)	**NC**	If two DDR memory chips are used this is the negative clock for the second chip and must stay connected. If DDR is not used leave open. (has internal pull up)
	VREF	I	Reference voltage		Must stay connected. (1.25V Typ. for SSTL-2 / 0.5 * VDD) (1.5V Typ. for SSTL-3 / 0.45 * VDD) Note: if the differential signaling intf. is not used, this pin must be connected to the memory IO's VDDR (3.3V or 2.5V)
	MEMVMODE	I	Voltage value for S(D/G)RAM chips.		Must stay connected. 0 or 0V for VDDR 3.3V 1 or VDDR for VDDR 2.5V Pin has internal pulldown for default of VDDR 3.3V
Zoom Video Port / External TMDS	ZV_LCDCNTL (3:0) ZV_LCDDATA(23:0)	I/O	Zoom Video Port **Or** TestBus output, **Or** JTAG control **Refer to pinout spec for pin name and signal name mappings**	**NC**	Leave open if not used. (have internal pull downs)
General Purpose IO	GPIO(13:0)	I/O	External TMDS, **Or** Serial ROM, **Or** Parallel ROM, **Or** Input TestBus, **And** straps **Refer to pinout spec for GPIO multiplexing and straps**	**NC**	Leave open if not used. (have internal pull downs)
LCD General Purpose IO	LTGIO(2:0)	I/O	Panel ID detection.	**NC**	Leave open if not used. (have internal pull downs)
LVDS	TXOUT_U0N	O	LVDS upper data channel 0 (-) .	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.

	TXOUT_U0P	O	LVDS upper data channel 0 (+)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_U1N	O	LVDS upper data channel 1 (-)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_U1P	O	LVDS upper data channel 1 (+)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_U2N	O	LVDS upper data channel 2 (-)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_U2P	O	LVDS upper data channel 2 (+)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_U3N	O	LVDS upper data channel 3 (-)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_U3P	O	LVDS upper data channel 3 (+)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXCLK_UN	O	LVDS upper clock channel (-)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXCLK_UP	O	LVDS upper clock channel (+)	**NC**	Only used in dual-channel LVDS mode. Leave open if not used.
	TXOUT_L0N	O	LVDS lower data channel 0 (-)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L0P	O	LVDS lower data channel 0 (+)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L1N	O	LVDS lower data channel 1 (-)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L1P	O	LVDS lower data channel 1 (+)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L2N	O	LVDS lower data channel 2 (-)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L2P	O	LVDS lower data channel 2 (+)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L3N	O	LVDS lower data channel 3 (-)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
	TXOUT_L3P	O	LVDS lower data channel 3 (+)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.

	TXCLK_LN	O	LVDS lower clock channel (-)	**NC**	This channel is used as the transmitting channel in sin channel LVDS mode. Leave open if not used.
	TXCLK_LP	O	LVDS lower clock channel (+)	**NC**	This channel is used as the transmitting channel in single channel LVDS mode. Leave open if not used.
LVDS PLL Power	LPVDD	I	Powering LVDS PLL macro **(1.8V)**		Power always required.
LVDS PLL GND	LPVSS	O	LVDS PLL macro ground pin		Power always required.
LVDS IO Power	LVDDR (x2)	I	Powering LVDS IOs. **(1.8V)**		Power always required.
LVDS IO GND	LVSSR (x2)	O	LVDS IO ground pin		Power always required.
External SSC	SSIN	I	External SSC Clock In (output from SSC)	**NC**	Leave open if not used. (has internal pull down)
	SSOUT	O	External SSC Clock Out (input to SSC)	**NC**	Leave open if not used. (has internal pull down)
Panel Control	DIGON	O	Controls Panel Digital Power On/Off	**NC**	Leave open if not used. (has internal pull down)
	BLONb	O	Control Backlight On/Off	**NC**	Leave open if not used. (has internal pull up)
Integrated TMDS	TX0P	AO	TMDS data channel 0 (+)	**NC**	Leave open if not used.
	TX0M	AO	TMDS data channel 0 (-)	**NC**	Leave open if not used.
	TX1P	AO	TMDS data channel 1 (+)	**NC**	Leave open if not used.
	TX1M	AO	TMDS data channel 1 (-)	**NC**	Leave open if not used.
	TX2P	AO	TMDS data channel 2 (+)	**NC**	Leave open if not used.
	TX2M	AO	TMDS data channel 2 (-)	**NC**	Leave open if not used.
	TXCP	AO	TMDS clock channel (+)	**NC**	Leave open if not used.
	TXCM	AO	TMDS clock channel (-)	**NC**	Leave open if not used.
	TPVDD	I	Powering TMDS PLL macro **(1.8V)**		Power always required.
	TPVSS	O	TMDS PLL macro ground pin		Power always required.
	TXVDDR(x2)	I	Power TMDS IOs. **(1.8V)**		Power always required.
	TXVSSR(x3)	O	TMDS IO ground pins		Power always required.
	DVIDDCDATA	I/O	DDC pin used for Panel ID; SDA functionality for TMDS	**NC**	Leave open if not used. (has internal pull up)

	DVIDDCCLK	I/O	DDC pin used for Panel ID; SCL functionality for TMDS	**NC**	Leave open if not used. (has internal pull up)
	HPD	I	panel detection	**NC**	Leave open if not used. (has internal pull down)
DAC (CRT)	R	AO	Red for monitor	**NC**	Leave open if no CRT.
	G	AO	Green for monitor	**NC**	Leave open if no CRT.
	B	AO	Blue for monitor	**NC**	Leave open if no CRT.
	HSYNC	I/O	Horizontal sync for Monitor This signal requires an on board TTL buffer (for eg. LS125)	**NC**	Leave open if not used. (has internal pull down)
	VSYNC	I/O	Vertical sync for Monitor This signal requires an on board TTL buffer (for eg. LS125)	**NC**	Leave open if not used. (has internal pull down)
	MONID(1:0)	I/O	MONID pins	**NC**	Leave open if not used. (have internal pull ups)
	VGADDCDATA	I/O	DDC pin / SDA for CRT	**NC**	Leave open if not used. (has internal pull up)
	VGADDCCLK AUXWIN	I/O I/O	DDC pin / SCL for CRT Special output pin for Apple monitors	**NC** **NC**	Leave open if not used. (has internal pull up) Leave open if not used. (has internal pull up)
	AVDD	I	DAC VDD **(1.8V)** Dedicated power for CRT DAC.		Power always required. Turn off DAC register way.
	AVSSN	O	DAC VSS Dedicated ground for CRT DAC.		Power always required.
	AVSSQ	O	Band Gap Ref. VSS		Power always required.
	RSET	O	Internal DAC reference		Must stay connected.
DAC2 (TV/CRT2)	Y_G	AO	SVID Y output for TV out, **Or** SCART Green output for TV out, **Or** Green for 2nd CRT Monitor	**NC**	Leave open if no TV out. When TV out is used, 75 ohm termination is needed on all outputs for proper TV detection.
	C_R	AO	SVID C output for TV out, **Or** SCART Red output for TV out, **Or** Red for 2nd CRT Monitor	**NC**	Leave open if no TV out. When TV out is used, 75 ohm termination is needed on all outputs for proper TV detection.
	COMP_B	AO	Composite Video for TV out, **Or** SCART Blue output for TV out, **Or** Blue for 2nd CRT Monitor	**NC**	Leave open if no TV out. When TV out is used, 75 ohm termination is needed on all outputs for proper TV detection.

	H2SYNC	I/O	Sync signal for TV SCART out, **Or** Horizontal Sync for 2nd CRT when TV out is not used.	**NC**	Leave open if not used. (has internal pull down)
	V2SYNC	I/O	Vertical Sync for 2nd CRT when TV out is not used.	**NC**	Leave open if not used. (has internal pull down)
	CRT2DDCCLK	I/O	DDC pin / SCL for second CRT or external TMDS Tx	**NC**	Leave open if not used. (has internal pull up)
	CRT2DDCDAT	I/O	DDC pin / SDA for second CRT or external TMDS Tx	**NC**	Leave open if not used. (has internal pull up)
	A2VDD	I	DAC2 VDD **(2.5V)**		Power always required. Turn off DAC register way.
	A2VDDQ	I	DAC2 Band Gap Ref. Voltage **(1.8V)**		Power always required.
	A2VSSQ	O	DAC2 VSS (quiet ground; use for Band Gap)		Power always required.
	A2VSSN	O	DAC2 VSS (noisy ground; used as current dump)		Power always required.
	R2SET	O	Internal Reference for second DAC		Must stay connected even TV out is not used
Test	TESTEN	I	Test mode enable	**PD**	Disable test mode
ROM	ROMCSb	O	BIOS ROM Chip Select	**NC**	Leave open if not used. (has internal pull up)
PLLs & XTAL	XTALIN	I	PLL Reference Clock or MXCLK source (14.318 - 29.4989 Mhz) (3.3V or 2.5V Input level)		Must stay connected
	XTALOUT	O	PLL Reference Clock	Refer to schematic	If oscillator is used as clock generator
	PVDD	I	Phase Lock Loop Power **(1.8V)**		Power always required.
	PVSS	O	Phase Lock Loop Ground		Power always required.
	MPVDD	I	Memory Phase Lock Loop Power **(1.8V)**		Power always required.
	MPVSS	O	Memory Phase Lock Loop Ground		Power always required.
Host Power	VDDP		**1.5V/3.3V** – PCI / AGP IO power for the AGP/PCI pins		Power always required.
Memory I/O Power	VDDR1 (memory)		**2.5V/3.3V (DDR/SDR)** IO power for the memory bus. Also I/O power for integrated memory in case of M6.		Power always required.

Memory core Power	VDDM		**2.5V/3.3V** Core power for integrated memory.		Power always required.
Memory die I/O Power	VDDQM		**2.5V (DDR only)** Memory die I/O power.		Power always required.
Memory clock Power	VDDRH		**2.5V/3.3V (DDR/SDR)** Dedicated power pin for memory clock pads. It should have the same voltage level as VDDR1		Power always required.
I/O Power	VDDR3 (other digital)		**3.3V** IO power for other pins		Power always required.
Core Power	VDDC		**1.8V** dedicated core power, provides power to the DDR-64/M6 internal logic		Power always required.
Memory clock Ground	VSSRH		Ground Dedicated ground pin for memory clock pads		Power always required.
I/O Ground	VSS		Ground		Power always required.

3 Power and Ground Considerations

3.1 Estimated Current and Power Consumption

The estimated current dissipation of each power input under various scenarios is detailed in the following table. Since these are estimated figures, the actual power consumption may vary slightly from the values shown.

Although RAGE Mobility-M6 can handle up to four display devices, the driver software may limit this to fewer than four displays since a digital display (LVDS/TMDS) and TV cannot share the same CRT controller.

Consequently, a typical worst case scenario on RAGE Mobility-M6 includes three displays (a CRT, a Digital Display Panel and a TV) all working together utilizing both the CRT controllers under the Dual-View setup. This is represented by Scenario 3 in the table. However, the figures shown may differ slightly under the following conditions:

- Using a larger panel (e.g., 1600x1200), or;
- Using an external-video capture device in addition to the other display devices already connected under scenario #3.

To obtain updated values contained in the following table, contact an ATI representative. Note that the following table contains estimated maximum and average power consumption based on measurements done on RAGE 6. The measurements for RAGE Mobility M6 will be published as they become available.

Table 3: Current Consumption

Item	Scenario #1	Scenario #2	Scenario #3
	Average case	Above average case	Worst case
	CORE + LVDS	CORE + LVDS + CRT DAC + TV DAC	CORE + LVDS + CRT DAC + TV DAC
Main regulator (VDDC, AVDD, TXVDDR, A2VDDQ) @ 1.8V			
Average	788.40 mA	1177.20 mA	1200 mA
Standby(D1 state)	107.83 mA	107.83 mA	107.83 mA
Suspend(D2 state)	TBD	TBD	TBD
PLL regulators (PVDD, LPVDD, TPVDD, MPVDD) @ 1.8V			
Average	38.30 mA	50 mA	50 mA
TVDAC regulator (A2VDD) @ 2.5V			
Average	0 mA	88.29 mA	90 mA
16 MB Internal Memory (VDDM, VDDQM) @ 2.5V/3.3V			
Average	194.04 mA	278.85 mA	330 mA
ASIC I/O's (VDDR1) @ 2.5V/3.3V			
Average	48 mA	48 mA	50 mA
GPIO's (VDDR3) @ 3.3V			
Average	19 mA	19 mA	20 mA
HOST I/O's (VDDP) @ 1.5V/3.3V			
Average	19 mA	19 mA	20 mA
Total Power	**2.22 Watts**	**3.37 Watts**	**3.56 Watts**

Item	Scenario #1 Average case	Scenario #2 Above average case	Scenario #3 Worst case
	CORE + LVDS	CORE + LVDS + CRT DAC + TV DAC	CORE + LVDS + CRT DAC + TV DAC

NOTES:

Scenario #1: Average case: single CRTC; LVDS only
Running 3D Winbench 2000, 1024x768x32, triple buffered, 16 bit Z buffer, single CRTC, single channel LVDS, at Memory clock (166 MHz) and Engine clock (166 MHz). Note: No CRT display is connected.

Scenario #2: Above average case: 3D Winbench but dual CRTC with TV-out
Running 3D Winbench 2000, 1024x768x32, triple buffered, 16 bit Z buffer, dual CRTC, TV-out, single channel LVDS, at Memory clock (166 MHz) and Engine clock (166 MHz). Note: CRT and TV are connected.

Scenario #3: Worst case: 3D Winbench, dual CRTC with TV-out, 32 bpp color depth
Running 3D Winbench 2000, 1024x768x32, double buffered, 16 bit Z buffer, dual CRTC, TV out, single channel LVDS, at Memory clock (166 MHz) and Engine clock (166 MHz). Note: CRT and TV are connected.

3.2 Layout Considerations

For optimal performance and system reliability, the RAGE MOBILITY M6 requires stable power supplies, and low-impedance power and ground returns. The above table shows the RAGE MOBILITY M6's demand for current for various power supplies. To ensure a successful design and implementation of a RAGE MOBILITY M6-based graphics subsystem, follow the layout guidelines in this chapter.

3.3 VIAs

To ensure a low-impedance path for power and ground nets (critical for reliable operation, use the following design measures:

- Use at least one via for each power pin, and one via for each ground pin.
- Keep the length of the trace (between any via and the associated power or ground pin) as short as possible (i.e., less than 0.025 inches).

3.4 Decoupling Capacitors

Use several groups of two capacitors (100nF and 10nF, or 0.1µF and 0.01µF) for each power supply–especially for VDDC (core power) and VDDR (I/O power).

Place all decoupling capacitors as close as possible to the RAGE MOBILITY M6. Place these groups of capacitors close to the appropriate power pads (i.e., a maximum of 100 mils away from the RAGE MOBILITY M6 chip).

Install at least one 22µF or 47µF tantalum capacitor on each of the following supplies: VDDP, VDDR1, VDDR3, VDDRH, VDDM, VDDQM and VDDC.

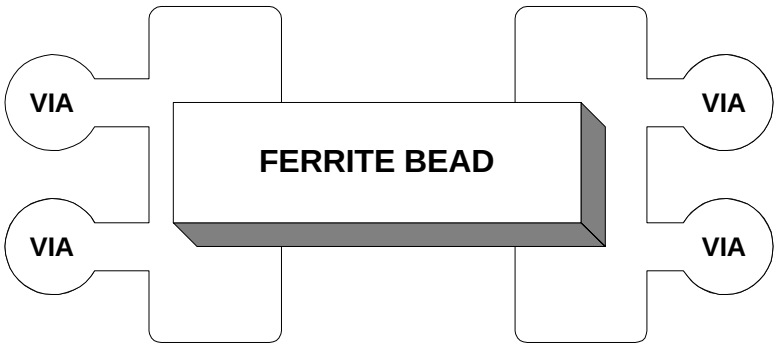


Figure 2: Typical Installation for a Ferrite Bead

3.5 Split VDDC Power Plane

Use a split VDDC power-island on the power plane. VDDC provides power to the core of the RAGE MOBILITY M6. VDDC has the highest peak current demand of all the power supplies.

To reduce the trace impedance, keep the width of the trace (routed from the VDDC regulator to the VDDC power island) greater than 50 mils.

Use at least three vias to connect this power trace to the VDDC power island.

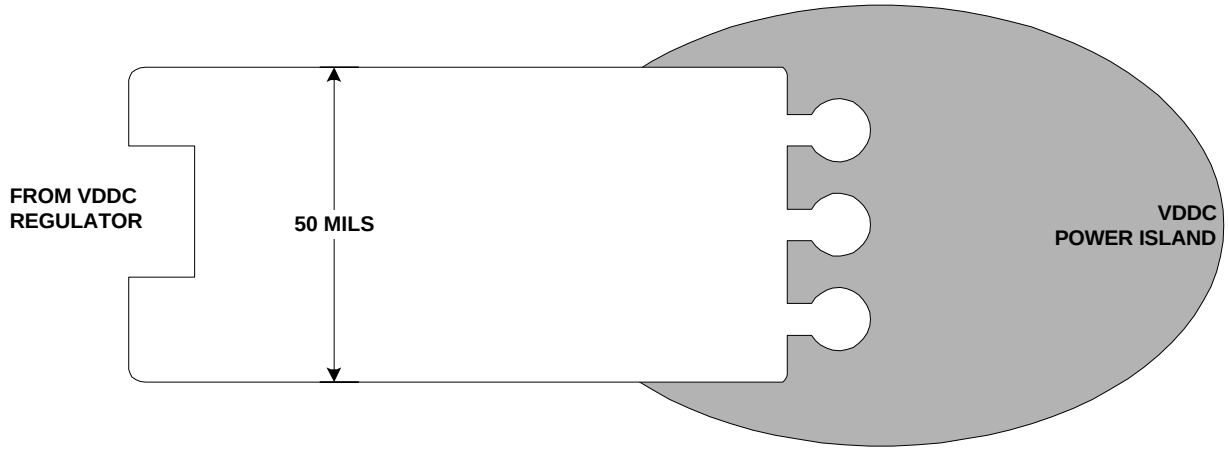


Figure 3: Split Power Plane

3.6 Separate Analog and PLL Power Supplies

It is strongly recommended to use a separate power regulator for each PLL. A stable PLL power supply ensures that the RAGE MOBILITY M6's internal and external clocks are stable and jitter free. Failure to provide a clean PLL power supply could result in intermittent system hangs or reduced display quality (especially at higher resolutions, refresh rates, or engine activity).

Keep all power supplies for the analog circuits separate from the PLL power supply. Use a separate analog-power island. Connect the AVDD power-island to the VDDC plane through a ferrite bead.

For power supplies related to the analog circuits and the power supply related to the PLL circuits, make sure that the width of the traces are greater than 15mils. These traces are routed from the regulator or ferrite bead to the power pins on the RAGE MOBILITY M6. The length of these traces should be less than 2.5 inches.

3.7 Signal Routing Considerations

When routing signals away from a BGA-type package, there is inevitably the need to use many vias. These vias could partially block both the power and ground planes in certain areas underneath the RAGE MOBILITY M6. This could lead to poor return current paths and reduce the thermal dissipation capabilities of the design.

It is recommended that the layout contain areas on all four sides of the RAGE MOBILITY M6 chip, which are free of vias. These areas should be at least 100 mil wide to provide uninterrupted access of the ground plane to the center of the BGA-type package where most of the ground balls are located.

3.8 Power sequence

The AGP I/O buffers in RV100 are designed to be able to automatically detect the power supply level on the AGP interface and configure output buffers based on the signal level that is expected. However, in order for that circuitry to work properly, there is special requirements in terms of power sequencing. This is only applicable for systems where VDDP is 3.3V (PCI, AGP 1X/2X systems). For systems where VDDP is 1.5V, there is no requirement regarding VDDP and VDDC power sequencing. For the best case scenario VDDC must be applied first and removed last. In some systems the core voltage (1.8V) is derived from a 3.3V voltage supply that feeds the I/Os. In this case the requirement is that the core voltage should follow the I/O voltage by a 0.8V margin until the core reaches the 1.6V voltage level. For example at the moment when the core voltage supply is 0.4V the I/Os voltage supply should not be higher than 1.2V. At the moment when the core voltage supply is 1.3V, the I/Os voltage supply can be no higher than 2.1V. At the moment when the core voltage supply is 1.6V, the I/Os voltage supply should not be higher then 2.4V. After the 1.6V voltage level is reached there are no more limitations.

For the ideal case the power sequencing scheme is outlined below. Also, in the following figure, the requirements for the case when core voltage is produced from

I/O voltage are illustrated. Please consult the schematics for the solution to this situation.

The power up sequence should proceed in descending order as shown below:

- VDDC (see discussion above)

3.3V Supply

- VDDR3
- VDDR1 (if connected to 3.3V)
- VDDP
- VDDM (if connected to 3.3V)
- VDDRH (if connected to 3.3V)

2.5V Supply

- VDDR1 (if connected to 2.5V)
- VDDM (if connected to 2.5V)
- VDDQM
- VDDRH (if connected to 2.5V)
- A2VDD

1.8V Supply

- TXVDDR
- LVDDR
- AVDD
- A2VDDQ
- PVDD
- MPVDD
- TPVDD
- LPVDD

The power down sequence is in reverse order.

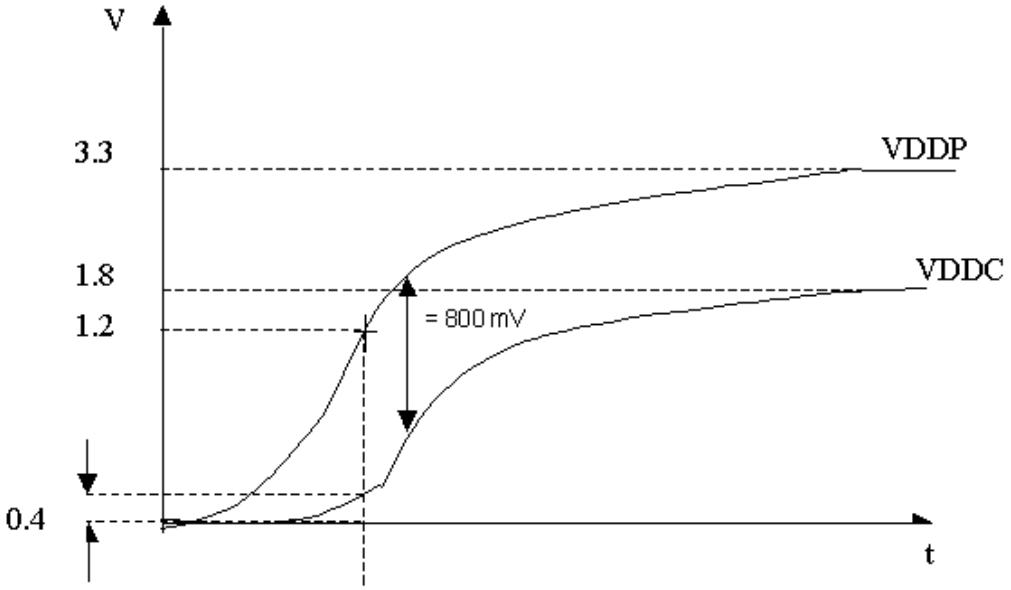


Figure 4 Power sequence when VDDC derives from VDDR

4 AGP Interface

4.1 Applicable Specifications

The AGP Interface is described by the Accelerated Graphics Port Interface Specification. These documents provide full specifications of the bus transaction protocols, and supply electrical, mechanical and configuration data for bus components and expansion boards. A useful companion documents is the AGP Platform Design Guide. Up-to-date copies of these documents may be obtained from the applicable sources.

4.2 Physical Connections

The RAGE MOBILITY M6's AGP Interface supports the AGP4X transfer protocol. The connection implements the set of signals required to carry out the AGP transactions utilizing the Sideband Addressing mechanism. The diagram below shows the signals comprising the AGP4X interface. Note however, that PCI, AGP1X and AGP2X cycles can still be run in this AGP4X design. The only difference is that the signaling is 1.5V as per the AGP4X specification.

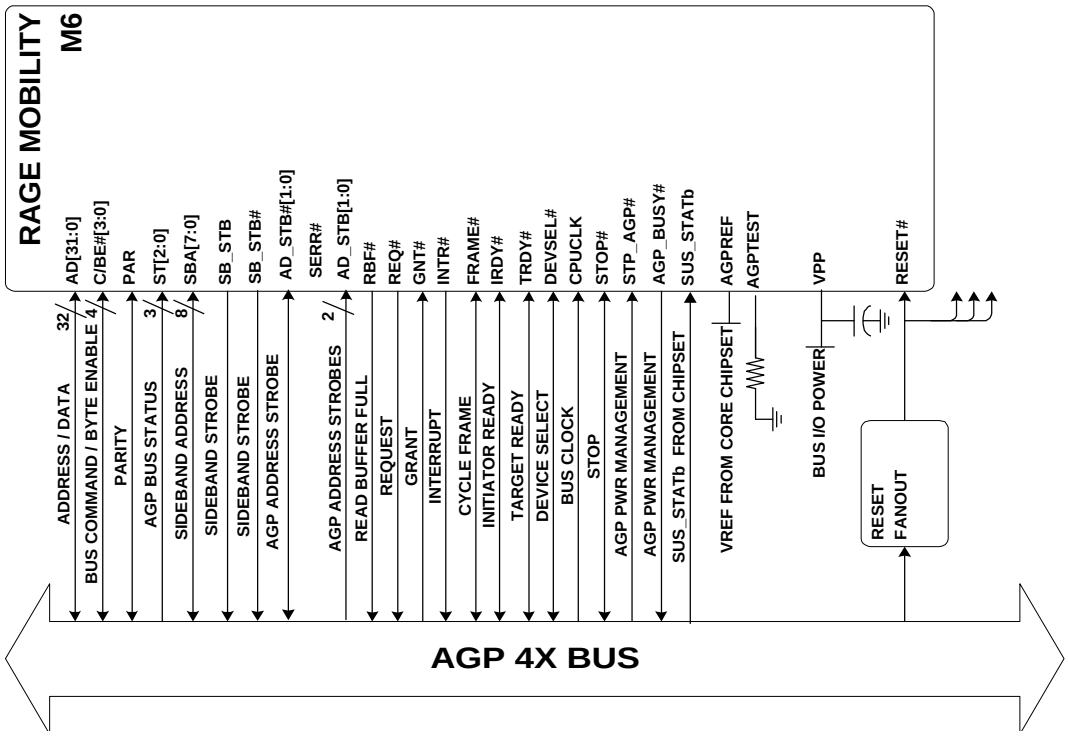


Figure 5: AGP Interface Block Diagram

4.3 Unused Signals

The AGP interface describes 20 signals beyond what PCI uses. The bus features supported by the Rage Mobility M6 controller require the implementation of these signals as shown below.

Signal Name	1x & 2x AGP interface		4x AGP interface		Description
SB_STB	SB_STB	1	SB_STB	1	Sideband Strobe
ST(2:0)	ST(2:0)	3	ST(2:0)	3	AGP Bus Status
SBA(6:0)	SBA(6:0)	7	SBA(6:0)	7	Sideband Address
RBFb	RBFb	1	RBFb	1	Read Buffer Full
AD_STB(1:0)	AD_STB(1:0)	2	AD_STB(1:0)	2	AGP Address Strobes
SB_STBb			SB_STBb	1	Sideband Strobe Bar
AD_STBb(1:0)			AD_STBb(1:0)	2	AGP Address Strobes Bar
AGPREF	AGPREF	1	AGPREF	1	AGP Reference Voltage
AGPTEST	AGPTEST	1	AGPTEST	1	AGP External Fixed Reference
AGP_BUSYb[3]	AGP_BUSYb	1	AGP_BUSYb	1	AGP Power Management
STP_AGPb[3]	STP_AGPb	1	STP_AGPb	1	AGP Power Management
SUS_STATb[3]	SUS_STATb	1	SUS_STATb	1	AGP Power Management

For PCI implementations, all the above pins remain unconnected.

You must connect STP_AGPb, AGP_BUSYb and SUS_STATb to 3.3V via a pull-up resistor. If the STP_AGPb or SUS_STATb signal is left unconnected, the controller may not respond to any AGP transaction.

4.4 Signal Levels and Electrical Requirements

4.4.1 Signal Levels

The voltage level of the AGP/PCI interface signals is determined by the bus type and signaling environment supported by the core chipset. The RAGE MOBILITY M6 can be configured for PCI or AGP operations. The RAGE MOBILITY M6 bus I/O's can be configured to handle all signaling environments supported by the controller.

In PCI implementations interface signaling is 3.3V (no 5V tolerance). In AGP platforms, interface signaling is 3.3V in AGP1x and AGP2x transfer modes and 1.5V in AGP4x transfer mode.

4.4.2 VDDP

VDDP is the power supply for the AGP bus interface. The RAGE MOBILITY M6 graphics subsystem uses VDDQ to power the controller's bus I/O ring. VDDQ is generated on the motherboard and made available to the graphics subsystem via the designated power rail on the connector. The VDDQ supply is connected to the

VDDP pins of the RAGE MOBILITY M6 controller and has value of 1.5V(AGP4x) or 3.3V(AGP1x, AGP2x).

In PCI designs, the PCI 3.3V will be connected to the VDDP pins.

Except for CLK, RSTb, INTAb, AGP_BUSYb, SUS_STATb and STP_AGPb all AGP interface signals scale with (and reference to) the VDDP power supply, which is 1.5V or 3.3V for RAGE MOBILITY M6. CLK, RSTb, INTAb, AGP_BUSYb, SUS_STATb and STP_AGPb are referenced to the 3.3V supply of the core chipset. Of these, INTAb and AGP_BUSYb are generated by the graphics controller. AGP_BUSYb has an external pull up to 3.3V outside of the RAGE MOBILITY M6. The RAGE MOBILITY M6 may chose to pull AGP_BUSYb low to 0V or tristate so that the pull ups bring the signal voltage to 3.3V. This is how 3.3V signaling is achieved while using a 1.5V supply to power the AGP I/Os.

4.4.3 VDDP Decoupling

The VDDP power plane and supply path are subject to switching currents. To reduce their effect, decoupling capacitors to ground must be used. Place these capacitors as close as possible to the VDDP pins of the controller. The values of the capacitors are specified in the reference schematics.

4.4.4 STP_AGPb and AGP Interface Power Management Output

In an ACPI-aware OS, OS will try to put the mobile system in low-power state whenever possible to conserve power.

When the mobile system decides to go to low-power state, it will assert STP_AGPb which is an input to the AGP graphics chip as a warning that system will not respond to PCI and AGP request from AGP graphics chip soon. Graphics chip should perform its internal management to prepare for that.

AGP graphics chip will assert its output AGP_BUSYb whenever it is busy and request the mobile system not to transit to a low-power state. However, this request is not always granted. The system may assert STP_AGPb even when AGP_BUSYb is asserted.

Rage Mobility M6 supports two different mobile AGP Busy specs; 1.61 version (for 440BX Intel platforms) and 0.1 version of Intel Solano2-M spec for Solano-2M based platforms. M6 has a register bit to control which platform it intends to support.

In an Intel 440 BX platform, AGP graphics chip needs only to implement STP_AGPb (input to graphics chip) and AGP_BUSYb(output from graphics chip). Pin SUS_STATb is not used and has to be pulled up to 3.3V. When STP_AGPb is asserted, the AGP chipset will not respond to AGP requests from graphics chip some

time later. Moreover, AGP clock will stop sometime later. The graphics needs to be prepared for that.

In an Intel Solano2-M platform, AGP graphics chip can also implement an optional input pin SUS_STATb. In this system, assertion of STP_AGPb only indicates that AGP chipset will stop responding to AGP requests shortly after, but does not indicate AGP clock will stop. Instead, assertion of SUS_STATb will indicate that.

You must connect STP_AGPb, SUS_STATb and AGP_BUSYb to 3.3V via a pull-up resistor. If the STP_AGPb or SUS_STATb signal is left unconnected, the RAGE MOBILITY M6 may not respond to any AGP transactions and may hang the system.

4.4.5 AGP Voltage Reference (AGPREF)

VREF is defined as the common switching level between a source and a receiver. It is a DC voltage reference signal used to set the input sense (switching) level on the AGP bus.

For AGP 4X 1.5V designs, both the graphics controller and the chip set are required to generate VREF and distribute it through the interface to their respective receivers. The VREF signal from the chipset must be connected to the AGPREF input pin of the RAGE MOBILITY M6 controller. Care should be taken when routing this signal to avoid noise pick-up. Keep away from other switching signals and pins to minimize cross talk.

To generate VREF for the chipset, use the simple voltage divider circuit as shown in the following figure. The divider is supplied by VDDQ (1.5V). The resistor ratio R1/R2 must be 1/1, and a decoupling capacitor must be connected on VREF. The VREF voltage divider circuit should be placed as close as possible to the AGP interface.

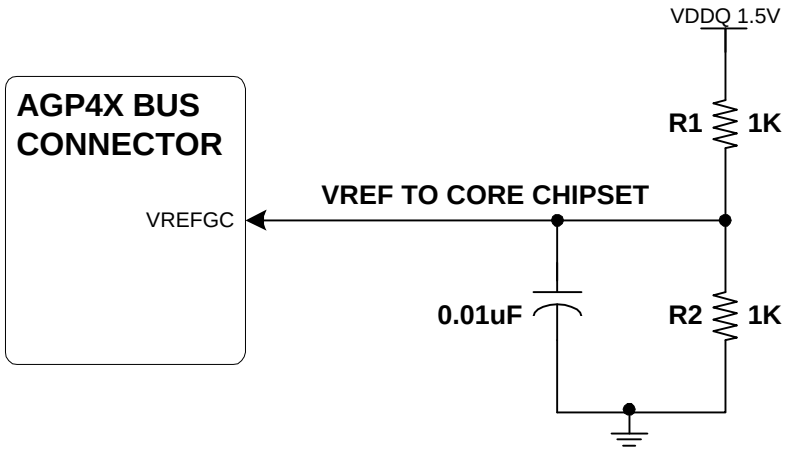


Figure 6: VREF Voltage Divider Circuit

For PCI, AGP1x and AGP2x designs with 3.3V signaling, this pin is not required and should be left unconnected.

4.4.6 AGPTEST

For AGP4x interface the RAGE MOBILITY M6 internal compensator uses this pin to determine and adjust the drive strength of the output drivers on the bus interface. To do this, the output buffer of the AGPTEST pad drives a current through an external resistor and measures the voltage. In AGP 1.5V implementations use a 45 Ohm +/- 1% resistor to connect AGPTEST to ground. If a 45Ω resistor is not available, a 47 Ohm +/- 1% resistor is a suitable alternate.

For PCI, AGP1x and AGP2x designs with 3.3V signaling, this pin is not required and should be no connect.

4.5 Layout and Routing Considerations

Component layout and routing of the interface signals must be carefully done to meet the timing and signal quality requirements of the AGP and PCI specifications. Design practices consistent with high-speed digital design should be followed. This includes thorough simulation of the interface to ensure compliance with flight times, skew and cross talk restrictions.

4.5.1 General Guidelines

Graphics subsystem components should be placed to minimize trace length, vias and interference with other signals. The pin out order of the RAGE MOBILITY M6 controllers has been optimized to match that of the core chipset. This alignment keeps overall trace length to a minimum, makes grouping of associated signals easier and helps in matching the trace lengths within the groups. All signals to the graphics

controller should follow the same order as the pin out of the connector.

4.5.2 AGP Address/Data and SideBand Strobes

You must group the AGP strobe signals and their complement counterparts with their associated data group. For example:

- ADSTB0/ADSTB0b with AD[15:0] and C/BEb[1:0]
- ADSTB1/ADSTB1b with AD[31:16] and C/BEb[3:2]
- SBSTB/SBSTBb with SBA[7:0]

Route the strobe signals in the middle of their respective groups. Locate the strobe signals to within ±0.5" of their respective groups.

4.5.3 Trace Length

The trace length for the AGP signal should be less than 3". This requirement is derived from the flight-time budget of 0.7ns.

The Bus Clock (PCICLK) trace should be less than the 0.6ns ±0.1ns flight-time requirement in the AGP specification.

Trace length can be calculated given the pertinent design parameters (such as number of layers, layer thickness, trace width, etc).

To calculate the propagation delay, use the following formula.

$$\text{Tprop (ps/in)} = 85\sqrt{(0.475\,\varepsilon r + 0.67)}$$

Where εr *is the relative permeability of the substrate*

Equation 1: Propagation Delay

For example: if strobe signal ADSTB0 is 2.5 inches, the trace lengths for signal groups AD[15:0] and C/BE[1:0] should be from 2.0 to 3.0 inches. The same rule applies to AD[31:16], SBA[7:0] and their respective strobes ADSTB1 and SBSTB.

4.5.4 Substrate Trace Length Report (AGP Section)

To design a useable motherboard that will be robust with the Rage Mobility M6, it is imperative that the trace lengths of all signals in the AGP section be taken due note of. The motherboard must meet the AGP trace length and routing requirements described in the Accelerated Graphics Port Interface Specification Rev. 2.0. In order to aid motherboard design, included below is the AGP section trace length report for

the Rage Mobility M6 ASIC. The total trace length is from the diepad to the ball of the ASIC. This dimension includes the length of the bondwire. It is suggested that all motherboard designers use these numbers to match trace lengths such that the skew between signals in any one of the three AGP groups is minimized. Ideally, all trace length skews within each group of AGP signals will be very close to zero millimeters.

M6/D6 Values

Table 4: Trace Lengths (8/16MB) - AGP Signals (Group 1)

Rage Mobility M6/D6 with Internal Hyundai memory
AGP Signals (Group 1)

Net Name	Ball #	Total Length (um)	Skew with AD_STB0 (um)	Skew with AD_STB0b (um)
AD(0)	D24	10375.09	230.86	1116.77
AD(1)	C26	11637.39	1493.16	2379.07
AD(2)	D25	11091.69	947.46	1833.37
AD(3)	D26	11525.62	1381.39	2267.30
AD(4)	E23	8715.6	1428.63	542.72
AD(5)	E25	11190.46	1046.23	1932.14
AD(6)	E24	9921.5	222.73	663.18
AD(7)	E26	11699.16	1554.93	2440.84
AD(8)	F26	11252.63	1108.40	1994.31
AD(9)	G23	10191.7	47.47	933.38
AD(10)	G25	9938.17	206.06	679.85
AD(11)	G24	9167.08	977.15	91.24
AD(12)	G26	10879.65	735.42	1621.33
AD(13)	H24	8719.4	1424.83	538.92
AD(14)	H26	11011.61	867.38	1753.29
AD(15)	H25	9670.64	473.59	412.32
CBEb(0)	F23	8742.35	1401.88	515.97
CBEb(1)	J25	9657.75	486.48	399.43
AD_STB(0)	F25	10144.23		***885.91***
AD_STBb(0)	F24	9258.32	***885.91***	
			MAX SKEW (ADSTB1 and ADSTRB1b) <=1 mm	
MIN		8715.60	47.47	91.24
MAX		11699.16	**1554.93**	**2440.84**
Difference between MAX and MIN trace length		2983.56	1507.46	
Average		10239.50	890.52	

Table 5: Trace Lengths (8/16MB)- AGP Signals (Group 2)

Rage Mobility M6/D6 with Internal Hyundai memory

AGP Signals (Group 2)

Net Name	Ball #	Total Length (um)	Skew with AD_STB1 (um)	Skew with AD_STB1b (um)
AD(16)	L23	9158.96	511.95	1502.49
AD(17)	L26	9857.1	1210.09	2200.63
AD(18)	L24	8426.67	220.34	770.20
AD(19)	M26	9900.62	1253.61	2244.15
AD(20)	M24	8039.73	607.28	383.26
AD(21)	N25	9018.02	371.01	1361.55
AD(22)	M25	9966.47	1319.46	2310.00
AD(23)	N26	9782.06	1135.05	2125.59
AD(24)	P23	7021.18	1625.83	635.29
AD(25)	P26	9857.18	1210.17	2200.71
AD(26)	P24	7681.88	965.13	25.41
AD(27)	R25	8997.38	350.37	1340.91
AD(28)	R24	7265.23	1381.78	391.24
AD(29)	R26	8895.85	248.84	1239.38
AD(30)	T23	7033.58	1613.43	622.89
AD(31)	T25	8867.65	220.64	1211.18
CBEb(2)	L25	9375.36	728.35	1718.89
CBEb(3)	N23	6876.85	1770.16	779.62
AD_STB(1)	P25	8647.01		***990.54***
AD_STRBb(1)	N24	7656.47	***990.54***	
			MAX SKEW (ADSTB1 and ADSTRB1b) <=1 mm	
MIN		6876.85	220.34	25.41
MAX		9966.47	**1770.16**	**2310.00**
Difference between MAX and MIN trace length		3089.62	1549.82	
Average		8616.26	933.37	

Table 6: Trace Lengths (8/16MB) - AGP Signals (Group 3)

Rage Mobility M6/D6 with Internal Hyundai memory

AGP Signals (Group 3)

Net Name	Ball #	Total Length (um)	Skew with SB-STB (um)	Skew with SB-STBb (um)
SBA(0)	W25	9094.69	222.68	573.42
SBA(1)	V24	7583.43	1288.58	937.84
SBA(2)	V26	9882.37	1010.36	1361.1
SBA(3)	V23	6941.11	1930.9	1580.16
SBA(4)	U26	9024.35	152.34	503.08
SBA(5)	U24	7539.77	1332.24	981.5
SBA(6)	T26	9884.39	1012.38	1363.12
SBA(7)	T24	7470.38	1401.63	1050.89
SB_STB	V25	8872.01		***350.74***
SB_STBb	U25	8521.27	***350.74***	
			MAX SKEW (ADSTB1 and ADSTRB1b) <=1 mm	
MIN		6941.11	152.34	350.74
MAX		9884.39	**1930.90**	**1580.16**
Difference between MAX and MIN trace length		2943.28	1778.56	
Average		8481.38	966.87	

P6 Values

Table 7: Trace Lengths on P6 - AGP Signals (Group 1)

Rage Mobility P6

AGP Signals (Group 1)

Net Name	Ball #	Total Length (um)	Skew with AD_STB0 (um)	Skew with AD_STB0b (um)
AD(0)	D24	10375.09	230.86	1116.77
AD(1)	C26	11637.39	1493.16	2379.07
AD(2)	D25	11091.69	947.46	1833.37
AD(3)	D26	11525.62	1381.39	2267.30
AD(4)	E23	8715.6	1428.63	542.72
AD(5)	E25	11190.46	1046.23	1932.14
AD(6)	E24	9921.5	222.73	663.18
AD(7)	E26	11699.16	1554.93	2440.84
AD(8)	F26	11252.63	1108.40	1994.31
AD(9)	G23	10191.7	47.47	933.38
AD(10)	G25	9938.17	206.06	679.85
AD(11)	G24	9167.08	977.15	91.24
AD(12)	G26	10879.65	735.42	1621.33
AD(13)	H24	8719.4	1424.83	538.92
AD(14)	H26	11011.61	867.38	1753.29
AD(15)	H25	9670.64	473.59	412.32
CBEb(0)	F23	8742.35	1401.88	515.97
CBEb(1)	J25	9657.75	486.48	399.43
AD_STB(0)	F25	10144.23		***885.91***
AD_STBb(0)	F24	9258.32	***885.91***	
			MAX SKEW (ADSTB1 and ADSTRB1b) <=1 mm	
MIN		8715.60	47.47	91.24
MAX		11699.16	**1554.93**	**2440.84**
Difference between MAX and MIN trace length		2983.56	1507.46	
Average		10239.50	890.52	

Table 8: Trace Lengths on P6 - AGP Signals (Group 2)

Rage Mobility P6

AGP Signals (Group 2)

Net Name	Ball #	Total Length (um)	Skew with AD_STB1 (um)	Skew with AD_STB1b (um)
AD(16)	L23	9158.96	511.95	1502.49
AD(17)	L26	9857.1	1210.09	2200.63
AD(18)	L24	8426.67	220.34	770.20
AD(19)	M26	9900.62	1253.61	2244.15
AD(20)	M24	8039.73	607.28	383.26
AD(21)	N25	9018.02	371.01	1361.55
AD(22)	M25	9966.47	1319.46	2310.00
AD(23)	N26	9782.06	1135.05	2125.59
AD(24)	P23	7021.18	1625.83	635.29
AD(25)	P26	9857.18	1210.17	2200.71
AD(26)	P24	7681.88	965.13	25.41
AD(27)	R25	8997.38	350.37	1340.91
AD(28)	R24	7265.23	1381.78	391.24
AD(29)	R26	8895.85	248.84	1239.38
AD(30)	T23	7033.58	1613.43	622.89
AD(31)	T25	8867.65	220.64	1211.18
CBEb(2)	L25	9375.36	728.35	1718.89
CBEb(3)	N23	6876.85	1770.16	779.62
AD_STB(1)	P25	8647.01		***990.54***
AD_STRBb(1)	N24	7656.47	***990.54***	
			MAX SKEW (ADSTB1 and ADSTRB1b) <=1 mm	
MIN		6876.85	220.34	25.41
MAX		9966.47	**1770.16**	**2310.00**
Difference between MAX and MIN trace length		3089.62	1549.82	
Average		8616.26	933.37	

Table 9: Trace Lengths on P6 - AGP Signals (Group 3)

Rage Mobility P6

AGP Signals (Group 3)

Net Name	Ball #	Total Length (um)	Skew with SB-STB (um)	Skew with SB-STBb (um)
SBA(0)	W25	9094.69	222.68	573.42
SBA(1)	V24	7583.43	1288.58	937.84
SBA(2)	V26	9882.37	1010.36	1361.1
SBA(3)	V23	6941.11	1930.9	1580.16
SBA(4)	U26	9024.35	152.34	503.08
SBA(5)	U24	7539.77	1332.24	981.5
SBA(6)	T26	9884.39	1012.38	1363.12
SBA(7)	T24	7470.38	1401.63	1050.89
SB_STB	V25	8872.01		*350.74*
SB_STBb	U25	8521.27	*350.74*	
			MAX SKEW (ADSTB1 and ADSTRB1b) <=1 mm	
MIN		6941.11	152.34	350.74
MAX		9884.39	**1930.90**	**1580.16**
Difference between MAX and MIN trace length		2943.28	1778.56	
Average		8481.38	966.87	

4.6 Guarding and Trace Pitch

To minimize cross talk, guard the Address Strobes, SideBand Strobes, and PCICLK. For these signals, the trace width to trace pitch ratio is 1:4. For all other signals, the ratio is 1:2 minimum.

4.6.1 Interface Control Signals

Cross talk is a problem that can affect signal levels and timing and may result in false triggering and data corruption. To minimize susceptibility to cross talk, follow good design practices.

However, some designs cannot achieve the desired level of immunity. For such designs, the signals FRAMEb, TRDYb, IRDYb, STOPb, DEVSELb, SB_STB, SB_STBb, AD_STB0, AD_STB0b, AD_STB1, AD_STB1b and SBA0 to SBA7 inclusive can be particularly susceptible. It is recommended that you install several series-resistor pads on these signals. For stable designs, these pads will be shorted.

However, if the design is slightly unstable, install a resistor into these pads (typical value could be 33Ω to 75Ω).

4.6.2 RESET

To start the initialization sequence of the system's devices, the system asserts RESET at power-up. All pins (including the bus interface signals) are tristated during its assertion. Keep RESET noise-free with clean and bounce-free edges.

Because of wide usage by the design, loading of RESET can become a problem. To add fan-out capability, use a discrete buffer. Place the buffer as close as possible to the bus connector. The following figure shows the proper configuration of the RESET buffer.

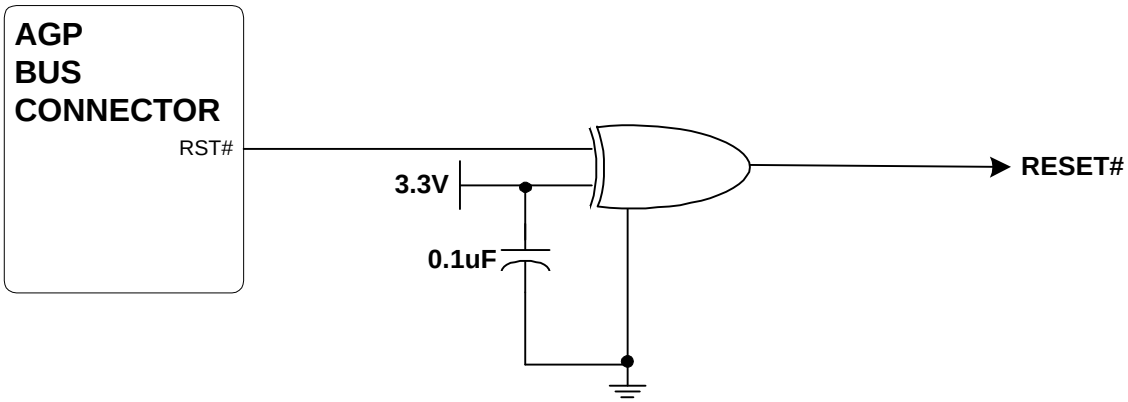


Figure 7: RESET Buffer Circuit

4.6.3 PCICLK

This is the clock for all transactions on the bus interface. Its frequency is 33 MHz for PCI 33 or 66MHz for PCI 66, AGP1X, AGP2X and AGP4X. The bus clock is connected directly to the PCICLK pin of the graphics controller. Make sure that the routing and impedance of the trace keeps the skew (between the controller and the system's chipset) less than 1ns.

4.7 Interface Configuration / Straps

The configuration of the AGP/PCI interface is handled through a group of straps implemented mostly on the GPIO (General Purpose Input/Output) lines. Among other configuration functions, these straps define the bus type, designate the clock source, and adjust the clock skew.

Two sets of straps are employed: external and ROM resident. The external straps are pull-up and pull-down resistors. The internal straps are stored inside the BIOS ROM (not applicable for motherboard design). All straps are read into the controller

during the assertion of RESET. Their value is then transferred and stored in system memory during the first PCI configuration cycle following the deassertion of RESET.

4.7.1 External Straps

For motherboard designs, leave GPIO[13:11] unconnected for proper opertion. This will prevent BIOS cycles from occurring. For add-in card designs, strap GPIO[13:11] to the proper values based on type of the EPROM that is used.

4.7.2 Internal Straps - GPIO Lines GPIO[13:0]

These straps are implemented on the GPIO[13:0] lines. After RESET, the straps are read and latched into the controller.

To set the '1' sense of the straps on the GPIO lines, use pull-up resistors to 3.3V (VDDR3). To set the '0' sense, leave straps open (they have internal pull-down).

4.7.3 VGA Disable - GPIO[7]

This strap is implemented on the GPIO[7] line. The default position is '0' (i.e. VGA-enable). With a pull-up in place, this strap disables the VGA portion of the controller. In this state, the controller will not be recognized as the system's VGA controller, but rather as a controller supporting extended display modes.

Use VGA-disable in dual-adapter configurations. In legacy environments (Win95 and previous), dual VGA adapters cannot co-exist on the same system. One of the two must have its VGA controller disabled by this strap. This strap is also losing its relevance as PC platforms begin to offer multi-display support through the operating system. A somewhat limited use of this strap is as a diagnostic tool to isolate VGA-related bugs.

4.7.4 ID Disable – GPIO[8]

This strap is implemented on the GPIO[8] line. For normal controller operation, the position of this strap is left open. To logically isolate the controller from the AGP bus, install a pull-up resistor to 3.3V. This "ID Disable" position disables the controller's response to AGP transactions.

The ID Disable strap allows the installation of a second AGP controller on the bus. At present, dual controllers cannot co-exist on the AGP bus. Thus, one controller must be logically removed when another is present. The ID Disable strap will disable one of two controllers in the case where one is already installed on the motherboard and the other is to be installed on the AGP slot.

4.7.5 Bus-configuration Straps - GPIO[6:4]

This straps are controlling the bus type, the clock PLL select and the IDSEL as shown in the following table.

Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66 MHz) strap.

Default is [000] – AGP4X.

Table 10: Bus Configuration Straps

BUSCFG 2 GPIO[6]	BUSCFG 1 GPIO[5]	BUSCFG 0 GPIO[4]	Description
0	0	0	1.5V bus, AGP4X, PLL clk, IDSEL=AD16
0	0	0	3.3V bus, AGP1X/2X, PLL clk, IDSEL=AD16
0	0	1	1.5V bus, AGP4X, PLL clk, IDSEL=AD17
0	0	1	3.3V bus, AGP1X/2X, PLL clk, IDSEL=AD17
0	1	0	1.5V bus, AGP1X/2X, PLL clk, IDSEL=AD16
0	1	0	3.3V bus, AGP1X/2X, PLL clk, IDSEL=AD16
0	1	1	1.5V bus, AGP1X/2X, PLL clk, IDSEL=AD17
0	1	1	3.3V bus, AGP1X/2X, PLL clk, IDSEL=AD17
1	0	0	PCI 66 MHz, PLL clk
1	0	1	PCI 33 MHz, 3.3V, REF clk
1	1	0	1.5V bus, AGP1X, REF clk, IDSEL=AD16
1	1	0	3.3V bus, AGP1X, REF clk, IDSEL=AD16
1	1	1	1.5V bus, AGP1X, REF clk, IDSEL=AD17
1	1	1	3.3V bus, AGP1X, REF clk, IDSEL=AD17

4.7.6 AGP Skew Straps - GPIO[1] and GPIO[0]

These straps allow for the adjustment of the phase between AGP 1X CLK and PCICLK as shown in the following table.

Table 11: AGP Skew

AGPFBSKEW 1 GPIO[1]	AGPFBSKEW 0 GPIO[0]	Skew Between AGP 1X CLK and PCICLK
0	0	PCICLK and AGP 1X CLK aligned
0	1	PCICLK one tap earlier than AGP 1X CLK
1	0	PCICLK one tap later than AGP 1X CLK
1	1	PCICLK two taps earlier than AGP 1X CLK

The alignment of PCICLK and AGP 1X CLK is theoretical only. Due to inherent path delay, PCICLK will always be slightly earlier than AGP 1X CLK.

AGP skew control is offered as a delay compensation feature. The AGP specification stipulates 1ns as the maximum skew between core chipset and controller. The design must adhere to this requirement in order to ensure reliable operation of the interface.

Ideally, the setting of the AGPFBSKEW straps should be ‘00’ (i.e. the aligned position). However, platform dependencies may dictate a small adjustment to compensate for errand loading and impedance factors.

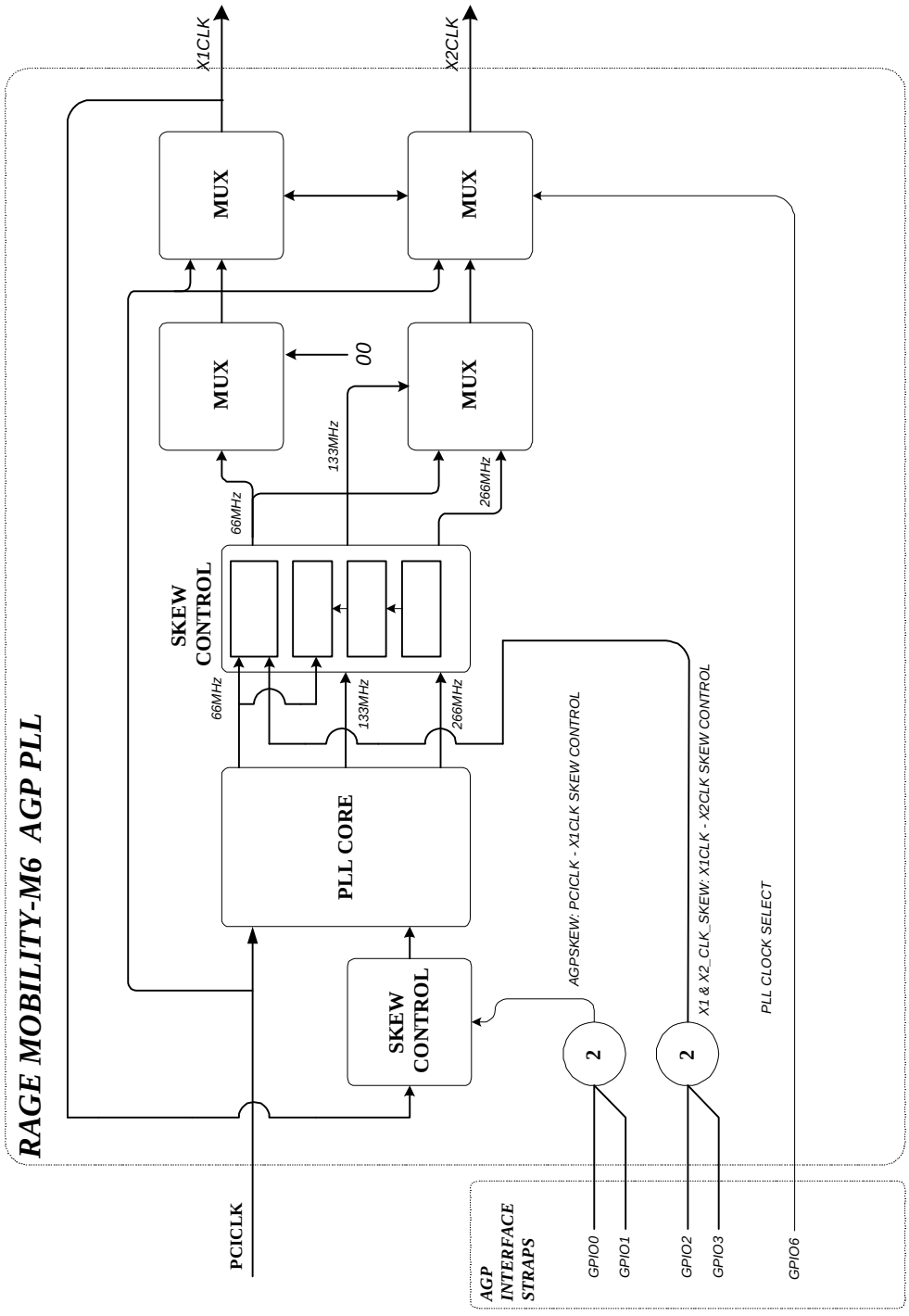


Figure 8: AGP Bus: Clock Selection and Skew Control

4.7.7 X1CLK_Skew Straps - GPIO[3] and GPIO[2]

These straps allow for the adjustment of the phase between X1CLK and X2CLK as shown in the following table.

Table 12: Clock Skew Straps

X1CLK_SKEW 1 GPIO[3]	X1CLK_SKEW 0 GPIO[2]	Delay Between X1CLK and X2CLK
0	0	X1CLK and X2CLK aligned
0	1	One tap delay between X1CLK and X2CLK
1	0	Two tap delay between X1CLK and X2CLK
1	1	Three tap delay between X1CLK and X2CLK

The alignment of X1CLK and X2CLK is theoretical only. Due to inherent path delay, X1CLK and X2CLK will always be slightly out of phase.

Skew control between X1CLK and X2CLK is offered as a delay compensation feature. Ideally, the setting of these straps should be ‘00’ (i.e. the aligned position). However, silicon process dependencies may dictate a small adjustment to compensate for errand loading and impedance factors.

4.7.8 ROMIDCFG Straps - GPIO[13:11]

If the graphic subsystem has no ROM attached, these straps serve for controlling the chip ID. In the event when a ROM is attached, these straps identify the ROM type as shown in the following table:

Table 15: ROMIDCFG straps

ROMIDCFG 2 GPIO[13]	ROMIDCFG 1 GPIO[12]	ROMIDCFG 0 GPIO[11]	Description
0	0	0	No ROM, CHG_ID = 0
0	0	1	No ROM, CHG_ID = 1
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Parallel ROM, chip ID’s from ROM
1	0	1	Serial AT25F1024, chip ID’s from ROM
1	1	0	Serial ST ROM, chip ID’s from ROM
1	1	1	Serial ISSI ROM, chip ID’s from ROM

Chip ID is based on CHG_ID strap (CHG_ID = ROMIDCFG(0) = GPIO[11]) and has the following options:

0 – default settings;

1 – reduced functionality (please check with ATI Marketing regarding details about reduced functionality).

5 PLL (Phase Lock Loop) Interface

5.1 Physical Connections

There are four dedicated pins used for the signaling, power and ground requirements of the PLL. These pins (XTALIN, XTALOUT, PVDD and PVSS) make up the external interface of the PLL.

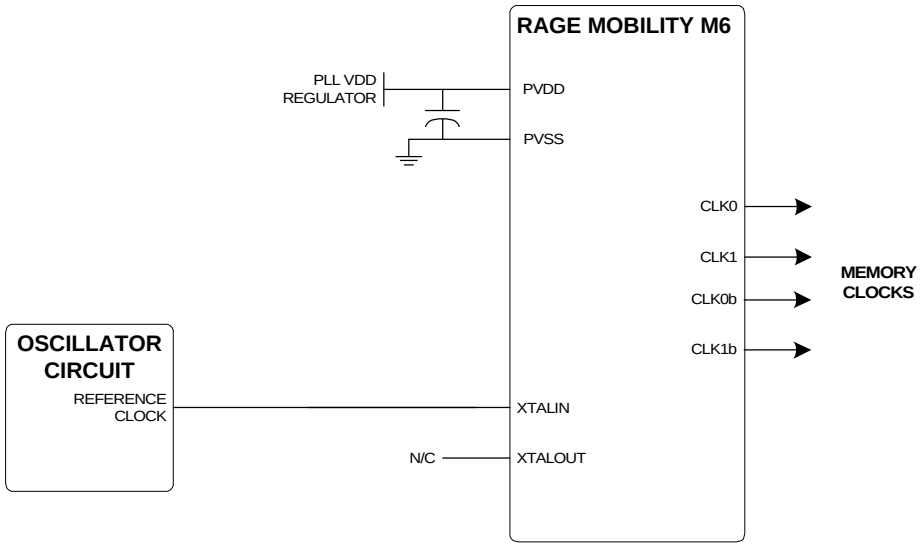


Figure 9: PLL Interface

The PLL is actually a group of five separate PLLs (Phase Locked Loops) and they are all implemented inside the controller. The sixth PLL is dedicated for memory clock generation and has separate power/ground pins (MPVDD/MPVSS). The following section provides a useful summary of the main clocks generated by the PLL.

5.2 Clock Overview

The RAGE MOBILITY M6 employs a multiple-output clock synthesizer to generate the internal and external clocks of the graphics subsystem. The synthesizer is commonly known as the PLL, but it actually consists of six distinct PLLs. Each PLL is dedicated to synthesizing the clocks of the controller's functional blocks as shown below.

Table 13: Clocks

PLL name	Generates Clocks For…
APLL	AGP bus interface
SPLL	2D, 3D, IDCT engines and registers
MPLL	Memory interface
PPLL	Primary display engine
P2PLL	Second display engine
TVPLL	TV OUT clock

The RAGE MOBILITY M6 PLL is capable of synthesizing any frequency up to 400MHz. It is programmable by video BIOS and by use of external straps. Refer to the applicable sections of this document for details on video BIOS and straps. The AGP PLL is special in that it is able to produce a 266 MHz clock.

WARNING. Clock frequencies are pre-set for optimal performance and reliability of the graphics subsystem. Re-programming the PLL in an attempt to improve graphics performance will result in unreliable operation or complete failure of the graphics subsystem.

5.3 Engine and Memory Clocks

The PLL generates the two major clocks: engine clock and memory-interface clock. The following definitions and characteristics apply to these clocks.

5.3.1 Engine Clock - SCLK

The SPLL generates this clock. The controller's internal-2D and 3D-engines use this clock. There are no external branches of SCLK. The video BIOS pre-sets this frequency. This clock is independent of the memory clock.

5.3.2 Memory Interface Clock - MCLK

This clock is used for the memory interface. The MPLL generates this clock. It is the clock for the internal 64-bit data bus. There is no external branch of this clock. However, the MPLL generates four related clocks for external use (CLK0, CLK0b, CLK1 and CLK1b).

These clocks are connected to controller output pins (CLK0, CLK0b, CLK1 and CLK1b) and used to drive the external memory interface in the case of P6 variant or looped back at the input pins CLK0_IN, CLK0b_IN, CLK1_IN and CLK1b_IN respectively for M6 or D6 variants.

The controller supports SDR and DDR memory types.

5.4 Engine and Memory Clock Frequency

The frequencies of the engine and memory-interface clocks are set for optimal performance and reliable operation of the graphics subsystem. All clock frequencies are programmed by video BIOS. The programmed values take effect upon initialization of the controller.

Typical settings for the engine clock are 133MHz, 150MHz, 166MHz, or 183MHz. Common settings for the memory-interface clock are 163MHz, 183MHz, or 200MHz. The clock frequency is determined by the speed of the memory devices and by the type of graphics controller.

The typical setting is 183MHz for the memory-interface (in case of P6) clock and 166MHz for the engine clock. In these configurations, the external memory clock runs at the same speed as the internal memory clock (i.e. the CLK/MCLK ratio is set to 1:1 such that MCLK = CLK = 183MHz for the above example). Currently, the maximum memory-clock frequency supported is 200MHz in both SDR and DDR modes (but check with ATI for the latest improvements).

5.5 Reference Clock Source: Crystal versus Oscillator

A crystal or an oscillator may be used to supply the reference clock. However, the reference clock from a crystal is more prone to noise pickup and this can lead to excessive jitter on the internal clocks.

An oscillator has higher immunity to noise and is thus a more reliable source for the reference frequency. Support is not provided for ATI RAGE THEATRE or ImpacTV as external TV encoder.

5.6 Reference Frequencies

The RAGE MOBILITY M6 PLL will synthesize all subsystem clocks from a single 27.0000 MHz reference frequency with ±50ppm accuracy.

5.7 Reference Clock Connections

The following diagrams show the different methods for connecting the reference clock to the controller in stand-alone designs.

5.7.1 Using RAGE MOBILITY M6 in Stand-alone Designs

For designs using oscillator box, the oscillator's reference clock is connected directly to the graphics controller's XTALIN pin. The XTALOUT pin remains unconnected, as shown in the following figure.

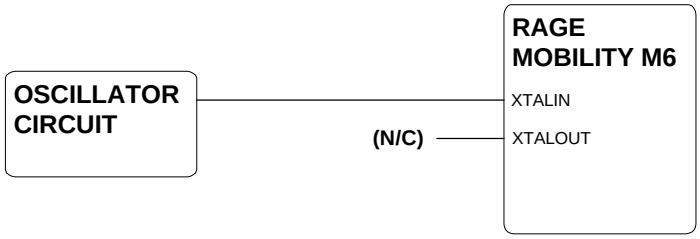


Figure 10: RAGE MOBILITY M6 with Oscillator

Although an oscillator or equivalent clock source is mandatory for RAGE MOBILITY M6 designs, provision could also be made for a crystal circuit (for possible cost reductions in the future), as shown in the following figure.

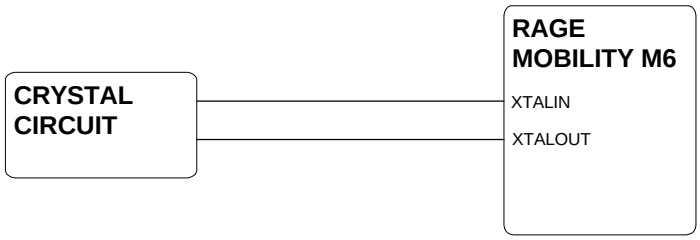


Figure 11: RAGE MOBILITY M6 with Crystal

5.8 Oscillator Circuit

The voltage tolerance of the XTALIN pin for the RAGE MOBILITY M6 is 1.8V. Since the design offers the option to use either a 3.3V or a 5V TTL oscillator, use a voltage divider along with a pull-up to 1.8V on the output. This will ensure a robust 1.8V swing on the reference clock signal. For circuit details, refer to the reference schematics.

5.9 Power and Grounding

The PLL interface requires dedicated power and grounding, and adequate de-coupling to ensure the generation of noise free, accurate clocks. Stable, jitter free clocks are essential to the functional integrity of the graphics subsystem. Noisy clocks may result in random and intermittent failures or reduced display quality, especially at higher resolutions and refresh rates.

5.9.1 PVDD, MPVDD, LPVDD, TPVDD

These are the power sources for the PLL logic. To ensure a clean power supply, provide a separate regulator. Connect decoupling capacitors between power and ground. Place these capacitors as close as possible to the power pad, a maximum of 100 mils away from the controller. To keep trace impedance low, the width of the power trace from the regulator to the pad should be greater than 15mils. The length of the trace should be less than 2.5".

5.9.2 PVSS, MPVSS, LPVSS, TPVSS

These are the dedicated ground pins for the PLLs. Keep them as bounce free as possible to avoid injecting noise into the PLL. Connect decoupling capacitors between power and ground.

6 Graphics Memory

6.1 Overview

The RAGE MOBILITY M6 incorporates a high-performance memory subsystem for processing and transferring images to the display. The memory controller arbitrates all transactions between the functional units and graphics memory. Among the features supported are programmable skews and delays, and SO-DIMM upgrade modules.

The controller supports an internal 32 or 64-bit data path (M6 or D6 variants) or an external 32 or 64-bit data path (P6 variant). The supported size of graphics memory is 64MB maximum and 8MB minimum. The memory types supported are SDR SDRAM, SDR SGRAM, DDR SDRAM, DDR SGRAM in a variety of configurations. For additional details about the various memory configurations, refer to the RAGE MOBILITY M6 Controller Specifications.

For RAGE MOBILITY M6 (8 MB) and D6 (16 MB) only integrated memory is supported. For RAGE MOBILITY P6 there is no integrated memory, the controller supports only external memory.

6.1.1 Support for SDR SDRAM Memory

The RAGE MOBILITY M6 supports main-memory Single Data Rate Synchronous DRAMs. The following is a list of features:

- LVTTL (3.3V) interface standard is supported
- 64-bit data bus interface, 1:1 mode up to a maximum 200MHz.
- 32-bit data bus interface, 2:1 mode up to a maximum 200 MHz
- 2 banks or 4 banks memories supported.

Table 14: Supported SDR SDRAM

2 Bank SDR DRAM Chips								
Type	**Data Rate**	**# of Rams**	**FB Size**	**Memory Width**	**# Physical Banks**	**Memory Config**	**Rank**	**Bank**
SDRAM - 1M x 16	SDR	4	8 MB	64-bit	1	512k x 16 x 2	1	2
4 Bank SDR DRAM Chips								
Type	**Data Rate**	**# of Rams**	**FB Size**	**Memory Width**	**# Physical Banks**	**Memory Config**	**Rank**	**Bank**
SDRAM - 4M x 16	SDR	4	32 MB	64-bit	1	1M x 16 x 4	1	4
SDRAM - 2M x 32	SDR	2	16 MB	64-bit	1	512k x 32 x 4	1	4
SDRAM - 2M x 32	SDR	4	32 MB	64-bit	2	512k x 32 x 4	2	4
SDRAM - 8Mx16	SDR	4	64 MB	64-bit	1	2M x 16 x 4	1	4

6.1.2 Support for SDR SGRAM Memories

The RAGE MOBILITY M6 supports graphics-memory Single Data Rate Synchronous Graphics RAMs. The following is a list of features:

- LVTTL (3.3V) interface standard is supported
- 64-bit data bus interface, 1-1 mode up to a maximum of 200MHz
- 32-bit data bus interface, 2-1 mode up to a maximum of 200 MHz
- No block-write feature
- 2 or 4 banks memories supported

Table 15: Supported SDR SGRAM

2 Bank SDR DRAM Chips								
Type	**Data Rate**	**# of Rams**	**FB Size**	**Memory Width**	**# Physical Banks**	**Memory Config**	**Rank**	**Bank**
SGRAM - 1M x 32	SDR	2	8 MB	64-bit	1	512k x 32 x 2	1	2
SGRAM - 1M x 32	SDR	4	16 MB	64-bit	2	512k x 32 x 2	2	2
4 Bank SDR DRAM Chips								
Type	**Data Rate**	**# of Rams**	**FB Size**	**Memory Width**	**# Physical Banks**	**Memory Config**	**Rank**	**Bank**
SGRAM - 2M x 32	SDR	2	16 MB	64-bit	1	512k x 32 x 4	1	4
SGRAM - 2M x 32	SDR	4	32 MB	64-bit	2	512k x 32 x 4	2	4

6.1.3 Support for DDR SDRAM Memories

The RAGE MOBILITY M6 supports graphics memory Double Data Rate Synchronous DRAMs. The following is a list of features:

- SSTL-2 (2.5V) interface standard is supported
- 64 bit data bus interface, 1-1 mode up to a maximum of 200 MHz
- 32 bit data bus interface, 2-1 mode up to a maximum of 200 MHz
- 2 or 4 banks memories supported

6.2 Memory for 64-Bit Interface

The following figure shows the external interface connections when the 64-bit wide memory path is used.

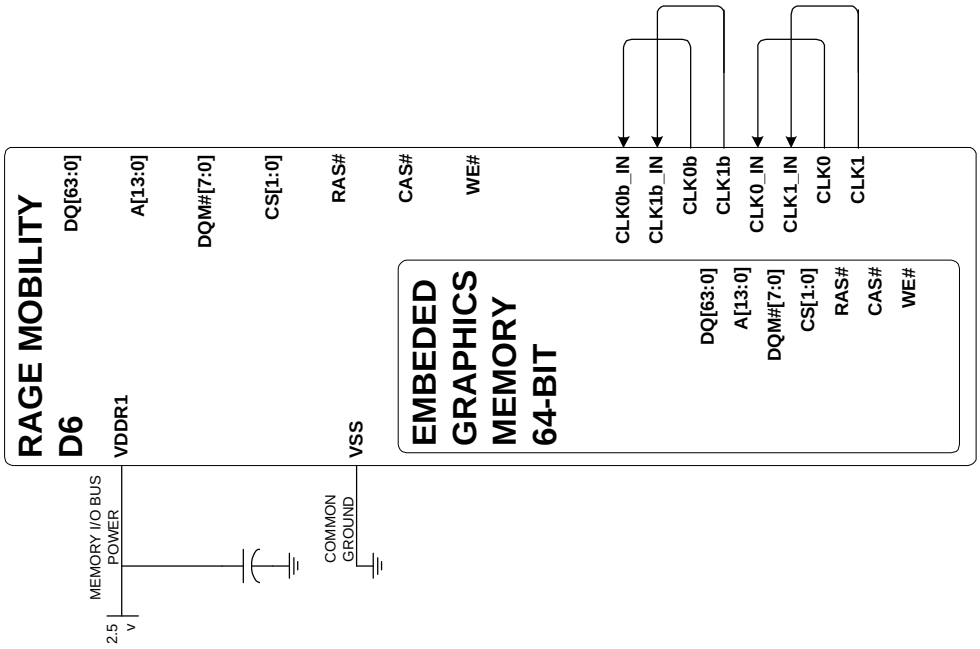


Figure 12: Graphics Memory Interface – 64 Bit

6.2.1 Memory Clocks

For 64-bit wide memory, CLK0b is used for the lower 32-bits, and CLK1b is used for the upper 32-bits.

6.2.2 Unused Pins

Except where indicated, unused pins should remain unconnected.

6.3 Memory for 32-Bit Interface

The diagram below depicts the interface connections with controllers that support 32-bit memory path.

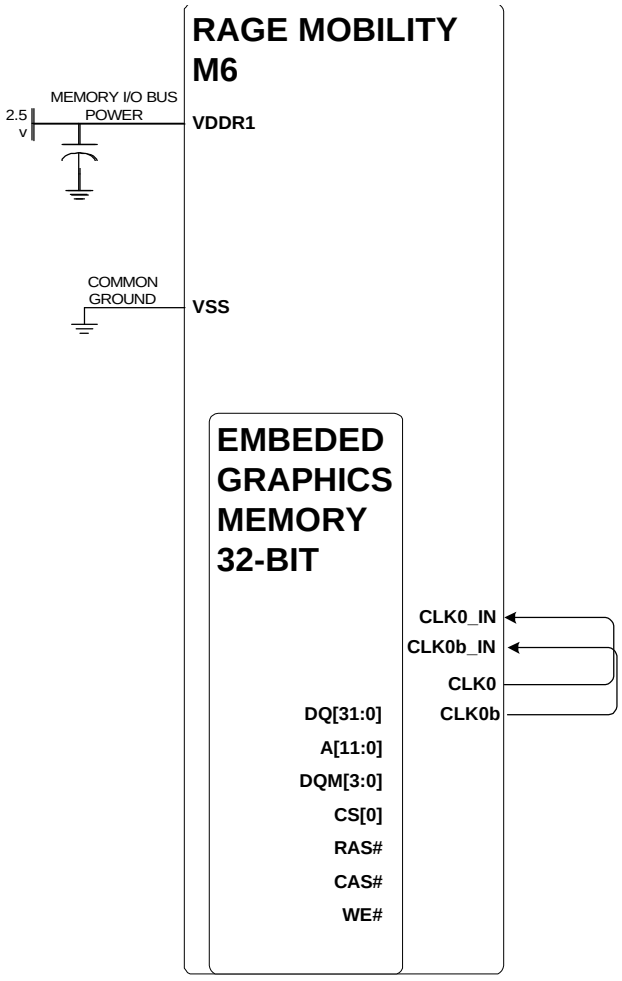


Figure 13: Graphics Memory Interface – 32 Bit

6.3.1 Memory Clocks

With a 32-bit wide memory, the lower 32 bits of the bus are connected to the memory devices. Thus, only CLK0 and CLK0b are used. CLK0 is fed back to CLK0_IN through some clock conditioning circuit. Same is done for CLK0b and CLK0b_IN.

For 32-bit memory, the supported upper-limit for the memory clock's frequency is 183MHz. The practical realization of this is a long-term goal that requires use of tighter specified devices along with minor adjustments to the silicon process.

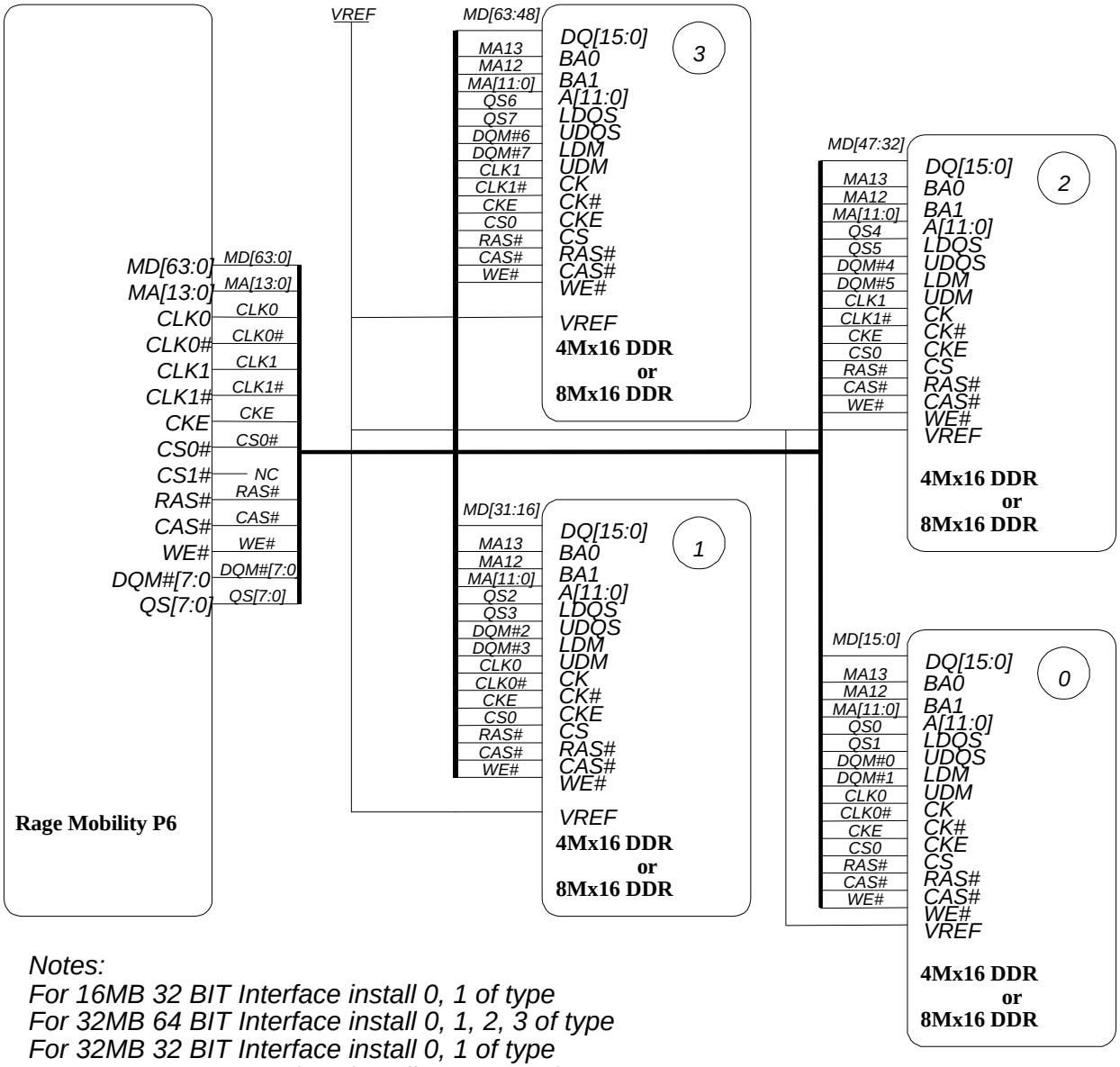
6.3.2 VDDR1

Power to the I/O pins of the memory bus is supplied through VDDR1. VDDR1 is connected to a 2.5V supply. The 2.5V should be sourced from a dedicated regulator.

6.3.3 Unused Pins

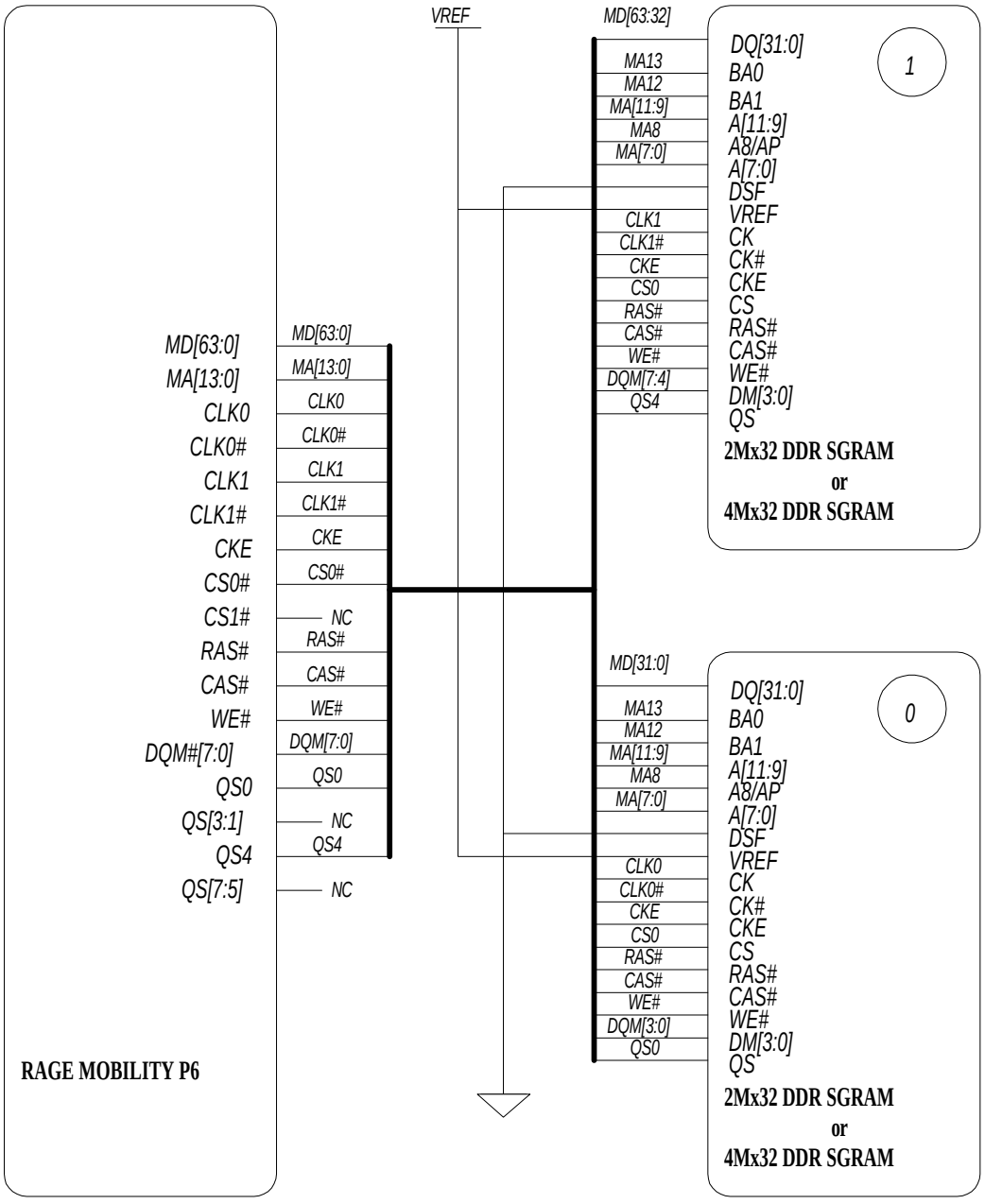
Except where indicated, unused pins remain unconnected.

6.4 Memory Configurations – P6



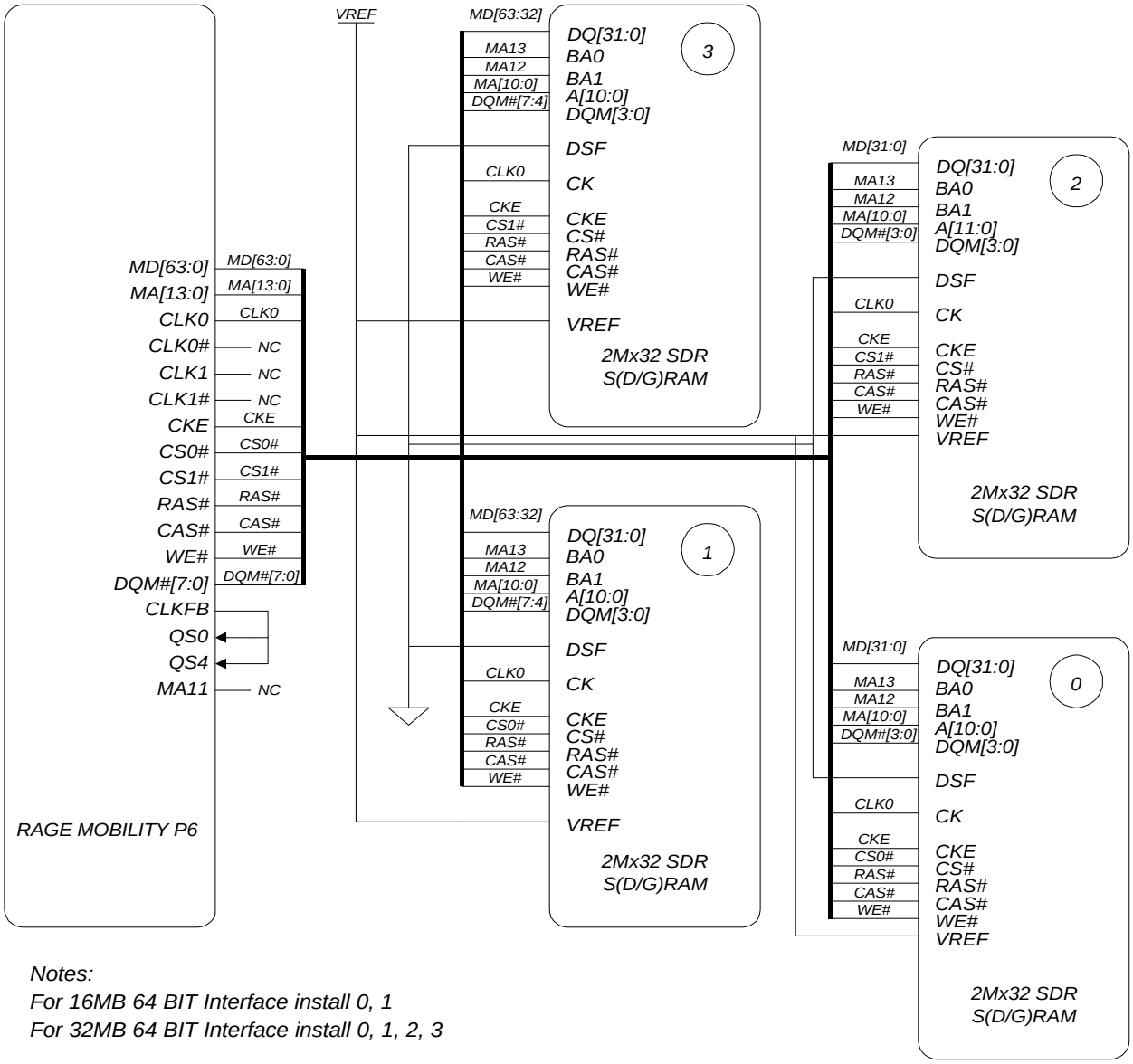
Notes:
For 16MB 32 BIT Interface install 0, 1 of type
For 32MB 64 BIT Interface install 0, 1, 2, 3 of type
For 32MB 32 BIT Interface install 0, 1 of type
For 64MB 64 BIT Interface install 0, 1, 2, 3 of type

Figure 14 DDR SDRAM Configuration



Notes:
For 8MB 32 BIT Interface install 0 of type 2Mx32
For 16MB 64 BIT Interface install 0, 1 of type 2Mx32
For 16MB 32 BIT Interface install 0 of type 4Mx32
For 32MB 64 BIT Interface install 0, 1 of type 4Mx32
**MA11 is needed only for the 4Mx32 part*

Figure 15: DDR SGRAM Configuration



Notes:
For 16MB 64 BIT Interface install 0, 1
For 32MB 64 BIT Interface install 0, 1, 2, 3

** DSF needed only for SGRAM parts*

Figure 16: SDR S(D/G)RAM configuration

6.5 Memory Layout Guidelines

This subsection provides layout guidelines and recommendations for the RAGE MOBILITY M6's memory interface that uses the DDR interface (either SDRAM or SGRAM devices).

Designers are encouraged to obtain ATI's IBIS models for the RAGE MOBILITY M6 drivers, and maintain their own models for the board and traces. Simulation is part of sound engineering practice and it should be employed to determine signal integrity, flight times, and skews.

6.6 Memory Clock Distribution and Layout

The source termination of memory clocks is mandatory. This termination must consist of a series-damping resistor and optional pull-up resistors and pull-down resistors. Place these resistors at the start of the clock trace, as close as possible to the controller, less than ~1 cm away from ASIC balls. Source termination will reduce reflections and make for a cleaner, more robust clock.

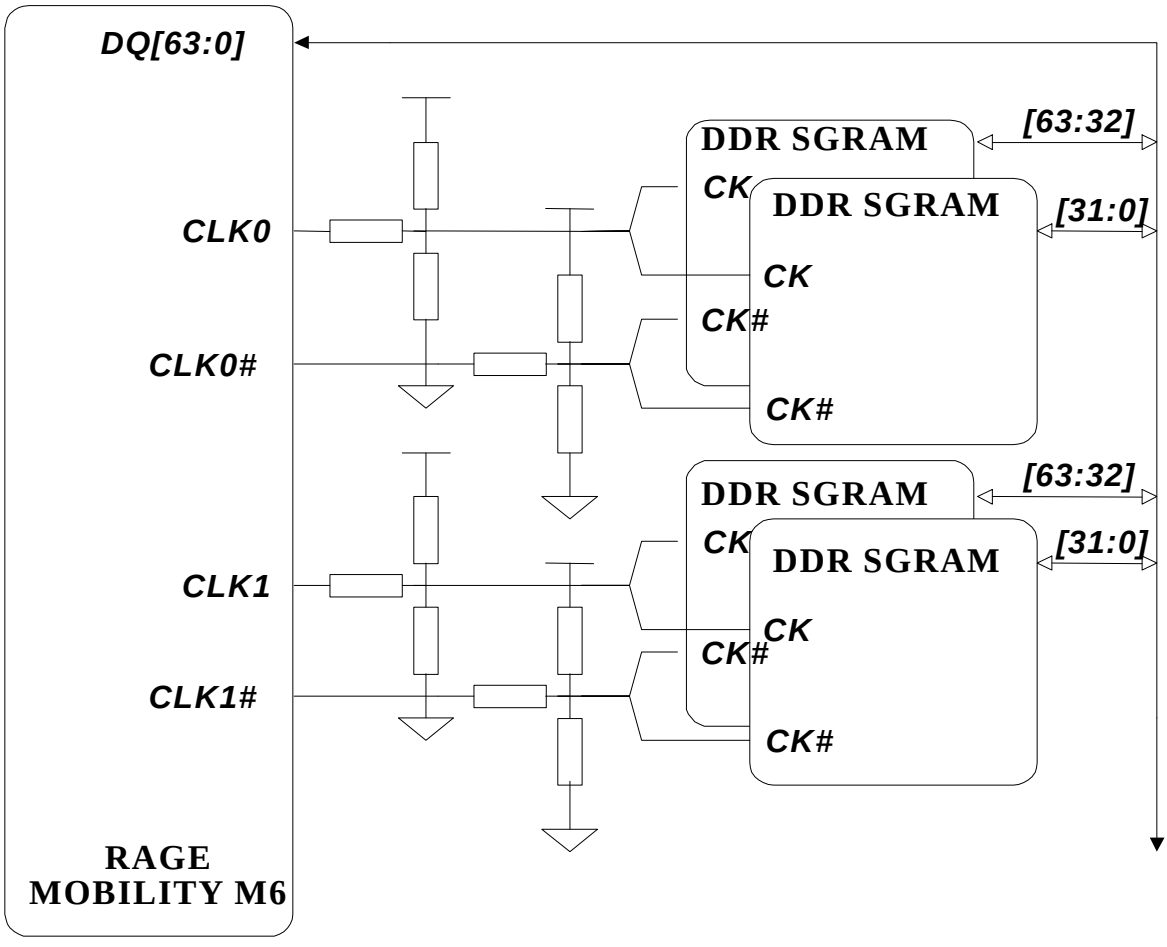


Figure 17: Memory Clock: Termination and Distribution for the 64-Bit DDR

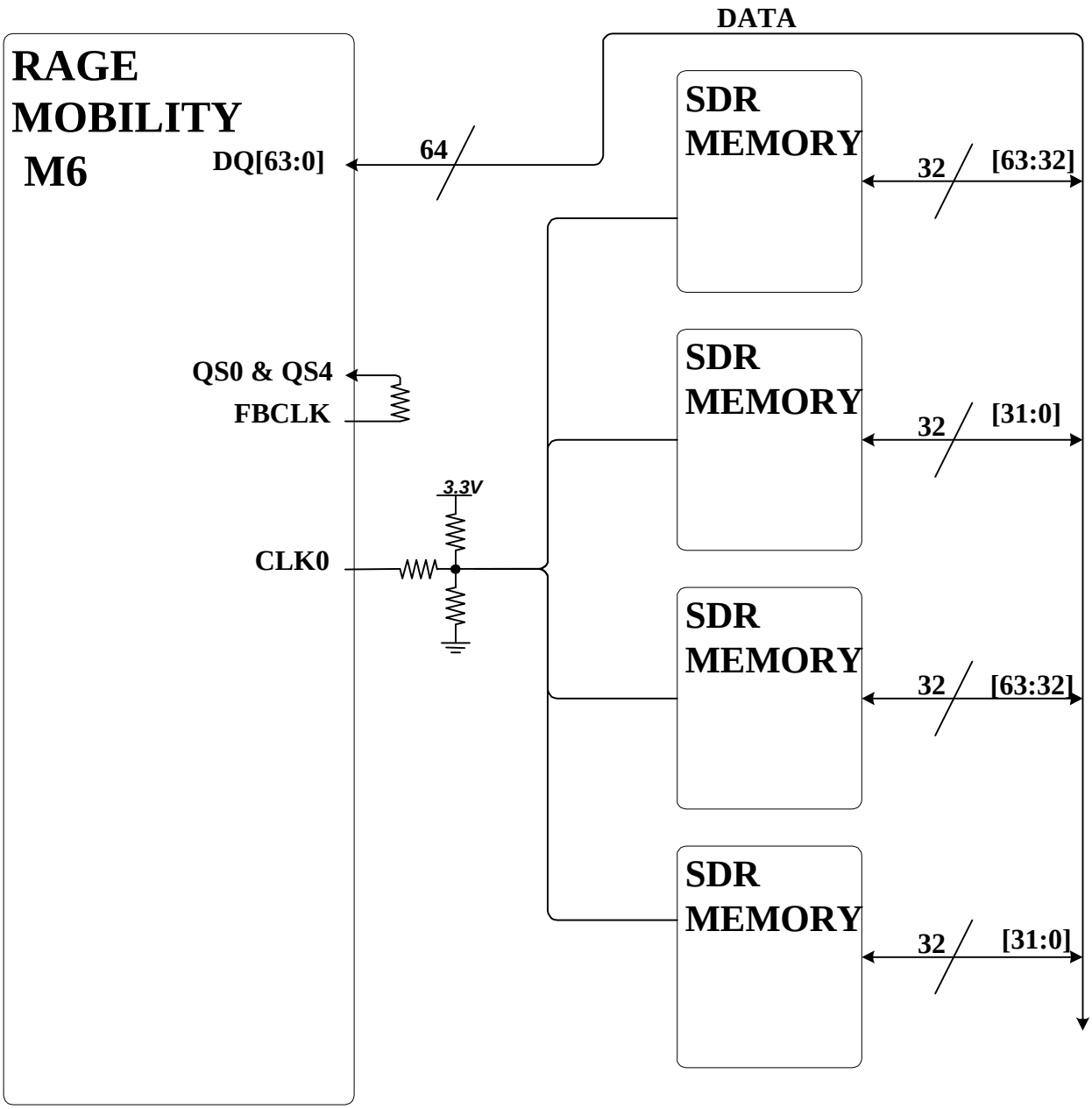


Figure 18: Memory Clock: Termination and Distribution for the 64-Bit SDR Interface

Clocking of the memory devices is carried out by the same clock. It is used to latch the data of the read cycle. For the 64-bit interface, CLK0 clocks both write/read transactions of the lower bus, bits[31:0], CLK1 clocks the transactions of the upper bus, bits[64:32]. The same convention is employed on the controllers that only support 32-bit interface. For these, CLK0 is used to clock both write and read

transactions. CLK1 is not required and should be left floating. It is important to have a clean signal at both the driver side pin and at the receiver side, since this signal is sensed and fed back internally. It is critical that this signal transitions smoothly through the threshold region (0.8-2.0V) and is glitch free.

Care should be taken when laying out the traces for CLK0 and CLK1. It is important to have a clean signal at the driver side pin (as well as at the receiver side) because this signal is sensed and fed back internally. It is critical that this signal transitions smoothly through the threshold region (around 0.8V-2.0V for LVTTL devices). The following pointers are recommendations for laying out the memory clocks.

- Route the memory clock signals away from other signals.
- Provide ground traces to guard the memory clocks. The ground traces should run the full length of both sides of the memory clocks.
- Preserve uninterrupted ground and powers plane. Locate them above and below the memory clocks.
- Optimize the memory layout for minimal trace lengths. Route the memory clocks in a modified star configuration (i.e. one trace should go to a position in the middle of all the memory chips, and equal length branches should proceed from the single point to each memory chip).
- Place the clock source termination as close as possible to the controller, less than ~1 cm away from ASIC ball.

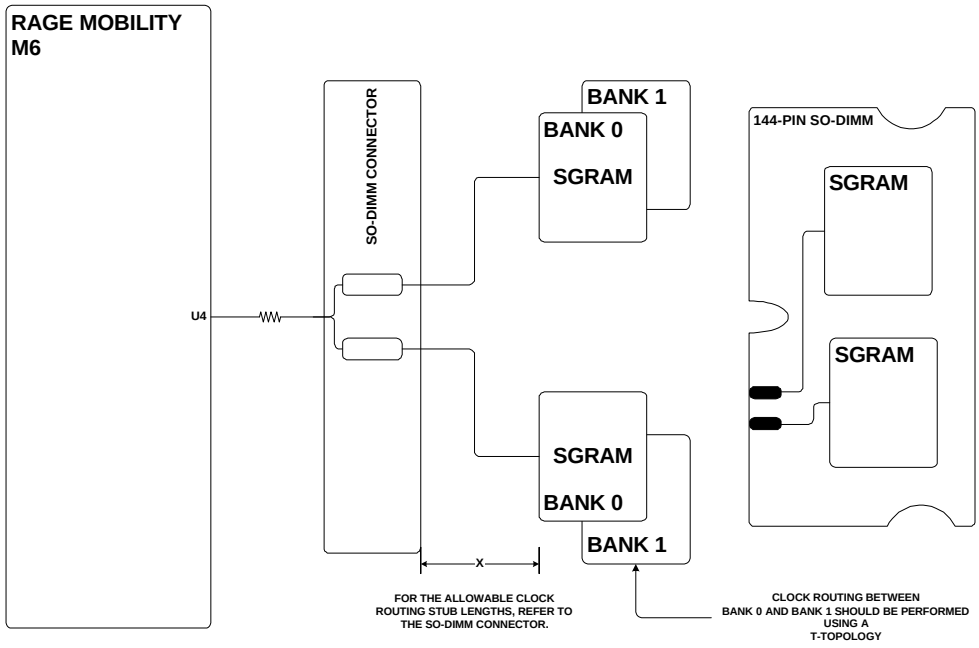


Figure 19: Memory Clock Routing

6.7 Memory Data, Address and Control Signal Layout

The following recommendations are for laying out the data, address, byte enable and other memory control lines.

- Lay out the memory devices in a topology that minimizes the trace length and any signal crossing.
- Group the memory control signals with their associated data group as much as possible.
- To minimize the effect of cross talk and ground bounce, use series resistors on all control signals, including byte enables. Place these resistors as close to the controller as possible, less than ~1cm away from ASIC balls. The same principle applies for data lines if an SODIMM connector is used. Use series resistors on all data signals. Place these resistors as close to the controller as possible, less than ~1cm away from ASIC balls.
- Place decoupling capacitors as close as possible to the power pads of the controller and the memory devices.
- Route data lines away from the rest of memory interface signal. Cross talk from read data changing in memory “command”, during setup time can cause command or address misinterpretation by memory itself.
- Data lines are bi-directional and their termination is not straight forward. For traces shorter than ~5cm, termination is not necessary. For traces between ~5-10cm, termination should be considered. Run simulation to see effects. If traces are longer than ~10cm, PCB should be redesigned.

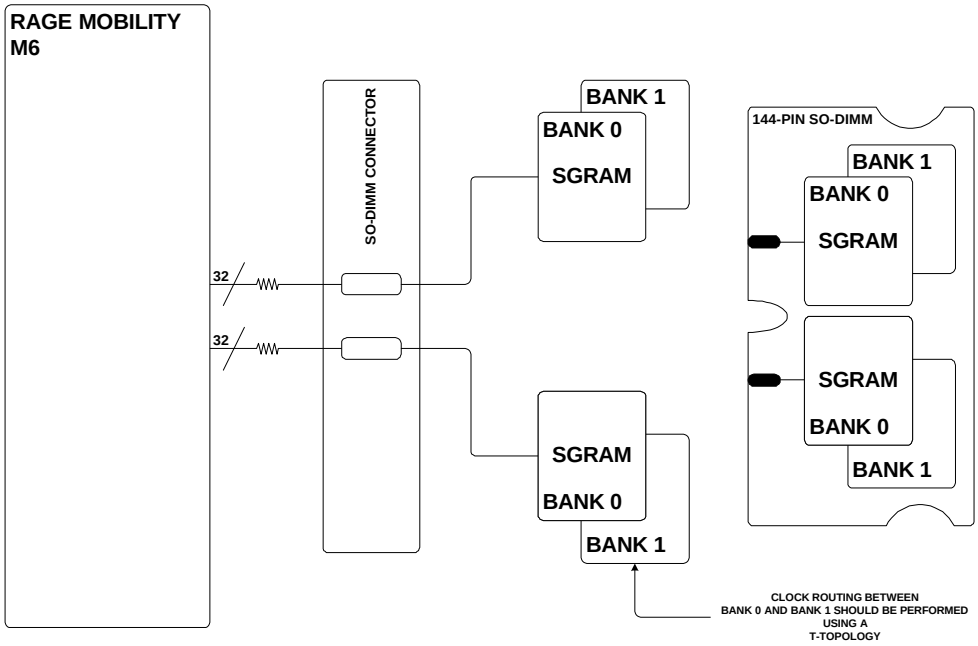


Figure 20: Memory Data Routing

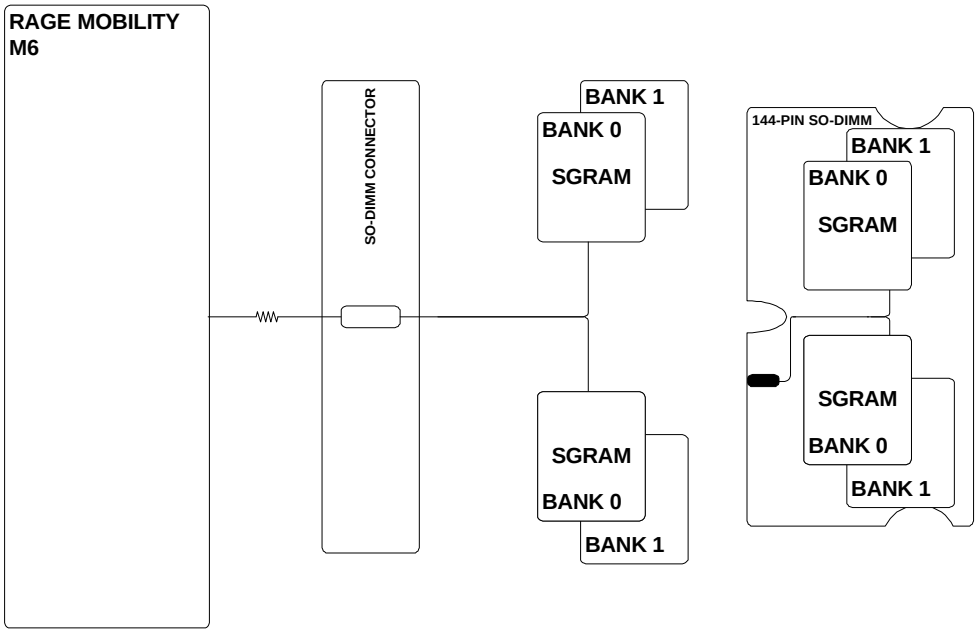


Figure 21: Address and Control Routing

6.8 DDR memories layout considerations

Most of mentioned layout considerations are only applicable for P6 ASIC (part without integrated memory). Only requirements regarding clock signals are applicable for M6/D6 variants.

6.8.1 General considerations

- If any signal is connected to more than one load, T topology routing should be necessary
- Maintain equal lengths on all traces that branch out as much as possible.
- Place all serial termination resistors as close as possible to their respective drivers.
- Place all Vtt termination resistors as close as possible to their respective signals. (If possible, It would be less than 0.1 inch)
- All by-pass capacitors should be placed as close to the related power pin as possible. The power and ground pins of the regulators should be double-bonded to the power or ground planes.
- Special care should be taken of routing memory clocks (CLK/CLK#) and data strobes (QS). They need to be adjacent to a ground or power layer. Avoid routing memory clock and strobe in parallel directions with traces on other layers.
- After routing is complete, all open areas are filled with GND or VDD(+2.5V). Basically, VDD area fills on the top layer and GND area fills on the bottom layer in case of signal1 – GND – VCC – signal2 stock-up. Furthermore, the area fills are connected to internal planes with one via for every 0.5 inch.
- The trace impedance need to be close to **60** ohm and routing ratio is to be **2:1**(A suggestion will be layout the traces as 8 mil with 8 mil spacing and then reduce the trace width to 5 mils)

6.8.2 The load conditions

Signals	16MB 2Mx32 SG	32MB 4Mx16 SD	16MB 2Mx32 SG	32MB 4Mx16 SD
DQ[63:0], DQM#[7:0], QS[7:0]	1 load	1 load	1 load	1 load
CLK[1:0], CLK#[1:0]	1 load	2 loads	1 load	2 loads
CS#[1:0]	2 loads	4 loads	2 loads	4 loads
RAS#,CAS#,WE#,CS#,CKE#,A[13:0]	2 loads	4 loads	2 loads	4 loads
Termination	Full	Full	Serial	Serial
The No. of memory devices	2 EA	4 EA	2 EA	4 EA

Table 16: Load conditions for memory signals

6.8.3 QS[7:0], DQM[7:0], MD[63:0]

- Special attention should be paid when Data Strobes QS[7:0] are routed. The routing ratio is to be 3:1(spacing : signal) at lest all over the way.
- Pull-up resistors for Vtt termination should be placed at the middle of lines because of bi-direction
- Data Strobes QS[7:0] should be in the middle with length of their associated data group. The data groups must be kept to within **+/- 0.2** inch of their respective strobe. For example, if the strobe is at 1.5inches, the data lines can be from 1.3 to 1.7 inches.
- The trace length mismatch of all data strobes(QS) should be less than **1** inch.
- Due to the limitation of having the round trip flight time in Read cycle, the length of QS plus CLK should be less than **1** clock cycle.

6.8.4 CLK0,CLK0#,CLK1,CLK1#

- They must be shielded with ground traces all over the way.
- For the layout of the pairs, the space **S** between the conductors of a pair should be kept to a minimum as shown below.(This means the routing ratio is to be 1:1)

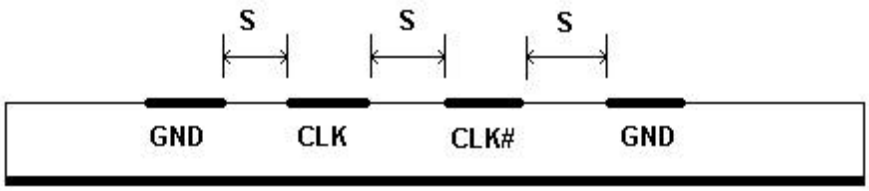


Figure 22: Clock pair shielding

6.8.5 RAS,CAS,WE,CS,CKE,A[13:0]

- It is highly recommended to maintain equal length on all traces that branch out as much as possible. It will effectively improve signal integrity and reduce the skew caused by the settling time.
- Control signal line length recommendation

Memory loading	Control signal line length
2 loads	**L**CLK – TBD inch < **L**CONTROL < **L**CLK + TBD inches
4 loads	**L**CLK – TBD inch < **L**CONTROL < **L**CLK + TBD inches

Table 17: Control signals line length

- In the following figure a practical case is detailed. c should be equal to d and also e = f = g = h.

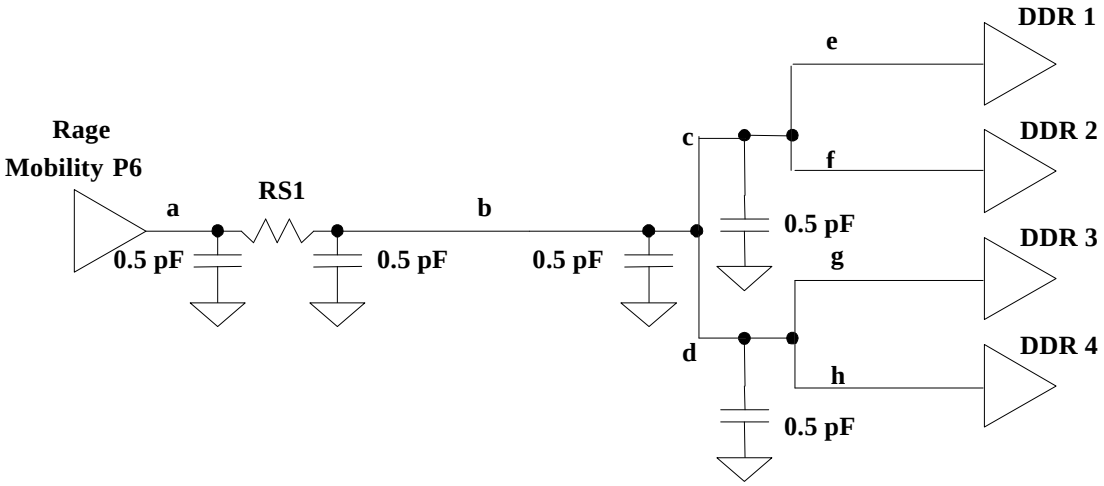


Figure 23: Practical case discussion for DDR layout

6.8.6 Vtt/Vref power Routing – Full termination only

- 6 layer PCB is strongly recommended for full termination design
- Vtt/Vref regulator must be located in the center of Vtt/Vref power trace(i.e., between channel A and B)
- Area fill of Vtt/Vref power line should be at least 500mils.
- One 0.1uF decoupling cap to GND per R-pack resistor and one 0.1uF cap to VDD(+2.5V) per R-pack. These are one after another.
- One 10~20uFcap to GND at either end of the island.
- Vref power line to each Memory and ASIC should be 25 mil wide trace and have own decoupling cap close to Vref pin.

6.8.7 Other guidelines

- In the case of DDR memories do use double terminations. The SSTL-2 documentation specifies two types of drivers – class I (8 mA) and class II (16 mA). A typical case of class II SSTL-2 DDR termination is illustrated in figure 24. For this case the drivers are stronger (16 mA) and data and strobe require 25 ohm (2 x 50 ohm) parallel termination as well as 50 ohm line impedance. Rage Mobility M6 uses class I drivers (8 mA) and the graphics memories also have class I drivers. In addition to that the series termination is built into the graphics controller therefore a 60 ohm line

impedance and 56 ohm parallel termination would be sufficient, as illustrated in figure 25. All termination resistors should be placed close to their respective drivers so install series resistors on the memory side. To summarize all of the above: put series termination close to ASIC on control, address and clock lines; put series termination close to memory on data, QS and DQM lines. For more details consult the schematics.

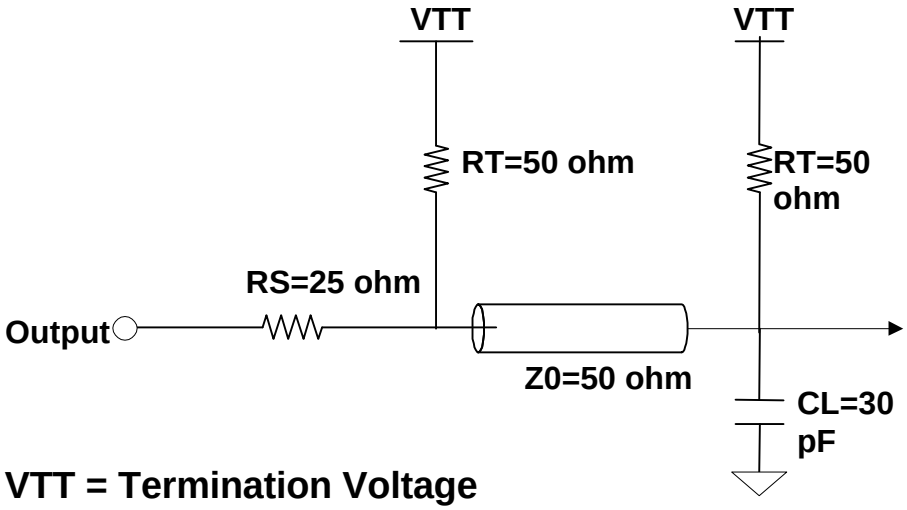


Figure 24: Class II SSTL-2 DDR termination

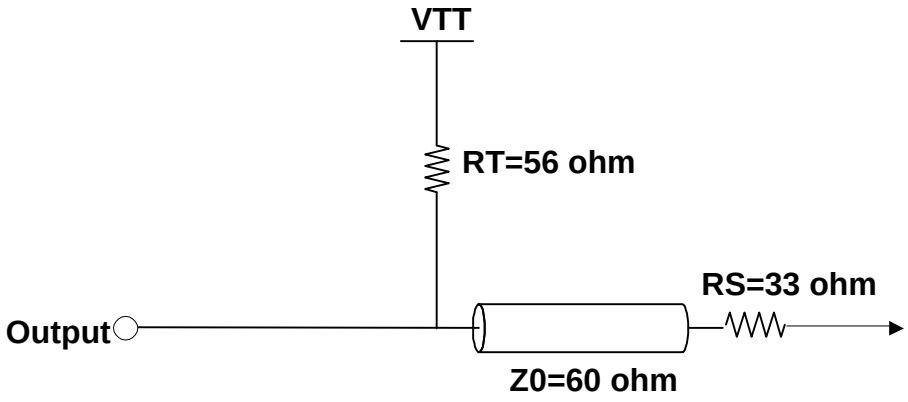
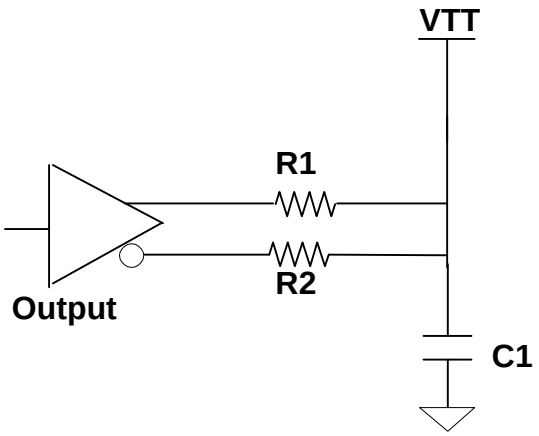


Figure 25: Rage Mobility M6 DDR termination

- The two resistor scheme figured below terminates all differential signals and all common mode signals on the clock lines and matters only if common mode signal is present. If both traces are perfectly equal, because of the differential nature of the scheme, the common mode noise would not exist and a single resistor termination would suffice. But for the case when the traces are not equal, a common mode noise is generated. For the case with single resistor termination, the common mode noise pulse returns to the driver where it finds a low impedance source, generating a big reflection. The reflected noise then travels to the receiver where it finds a single resistor termination. Because the common mode noise presents the same voltage on both traces, the single resistor terminator draws zero current, acting as an open circuit and generating another big reflection. The common mode noise then bounce back and forth between driver and receiver for a long time.
- If the trace delay equals one quarter of the clock period bad things can happen. In that case the common mode noise builds and superimposes on itself, cycle after cycle, magnifying the common mode input range and radiated emissions.
- For the scheme below these things don't happen. The capacitor need be only large enough to hold its charge steady during the brief interval between the arrival time of the two differential signals.



VTT = Termination Voltage

Figure 26: Independent termination for clock signals

7 Video BIOS

7.1 Overview

The RAGE MOBILITY M6's video BIOS initializes the graphics controller to a known state at system startup. The system startup sequence includes calls to the video BIOS, which in turn invokes its own functions and routines to setup the operational parameters of the graphics subsystem. The video initialization sequence includes: setup of display modes, initialization of the multimedia interface and PCI configuration space, and reading of straps.

The RAGE MOBILITY M6's video BIOS interface supports two different types of serial EEPROM; AT25F1024 or NX25F011 ROM and parallel flash BIOS AT49LV001. The interface can address up to 128K locations. Thus, either 64K or 128K devices can be used. Currently, all RAGE MOBILITY M6 features and functions can fit in a 64K device.

For add-in card designs, serial or parallel EEPROMs are required. For motherboard designs, a discrete device is not required, because the video BIOS is routinely integrated into the system BIOS. The drawback for these implementations is that the constraints in the system's BIOS space usually limits the size of the video BIOS to 32K. This restriction results in the exclusion of non-essential functions and features.

7.2 BIOS Interface

The GPIO pins are used to implement the video BIOS interface. The design will work with a serial or parallel EEPROM. The interface supports device densities of 64KB or 128KB. Selecting a device type and density is a tradeoff between cost and programming considerations.

7.2.1 Configuration for Serial EEPROM

The serial EEPROM interface is available for the RAGE MOBILITY M6 designs, as shown in the following figure.

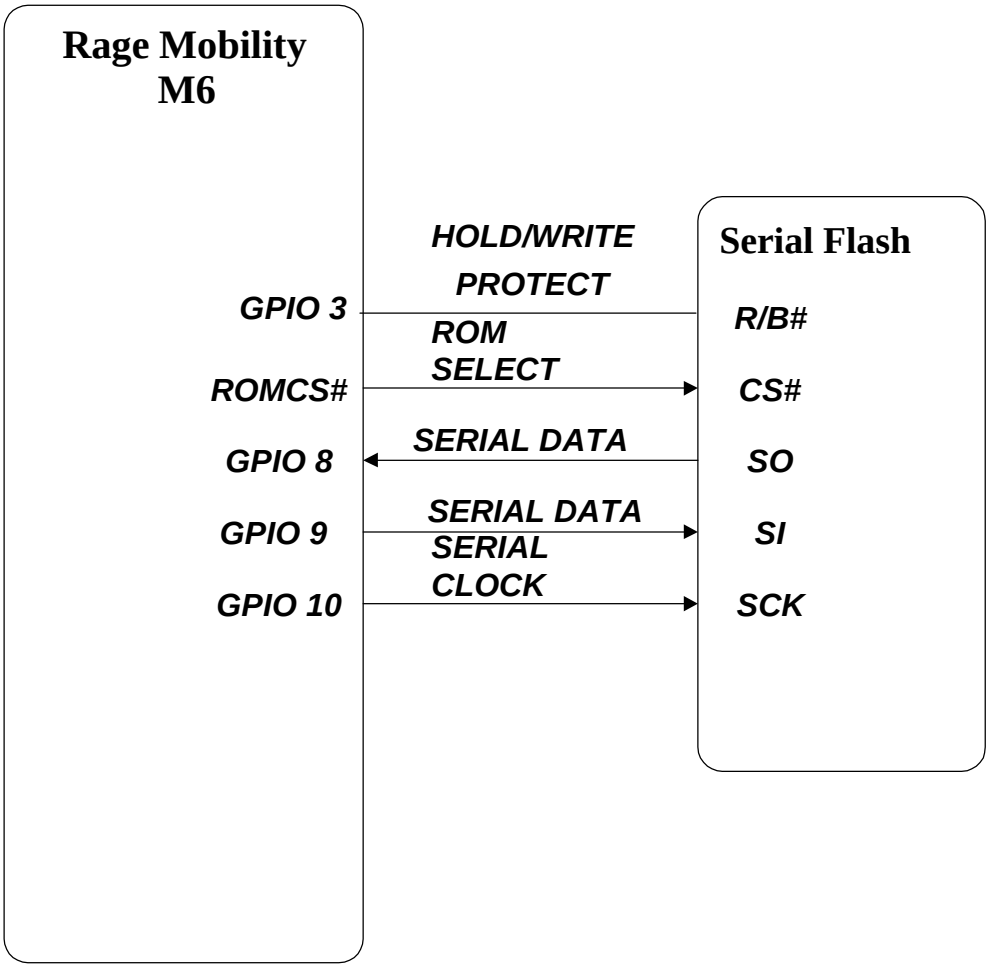


Figure 27: BIOS Interface – Serial EEPROM Configuration

7.2.2 Configuration for Parallel EEPROM

The parallel flash BIOS interface is also available for the RAGE MOBILITY M6 designs, as shown in the following figure:

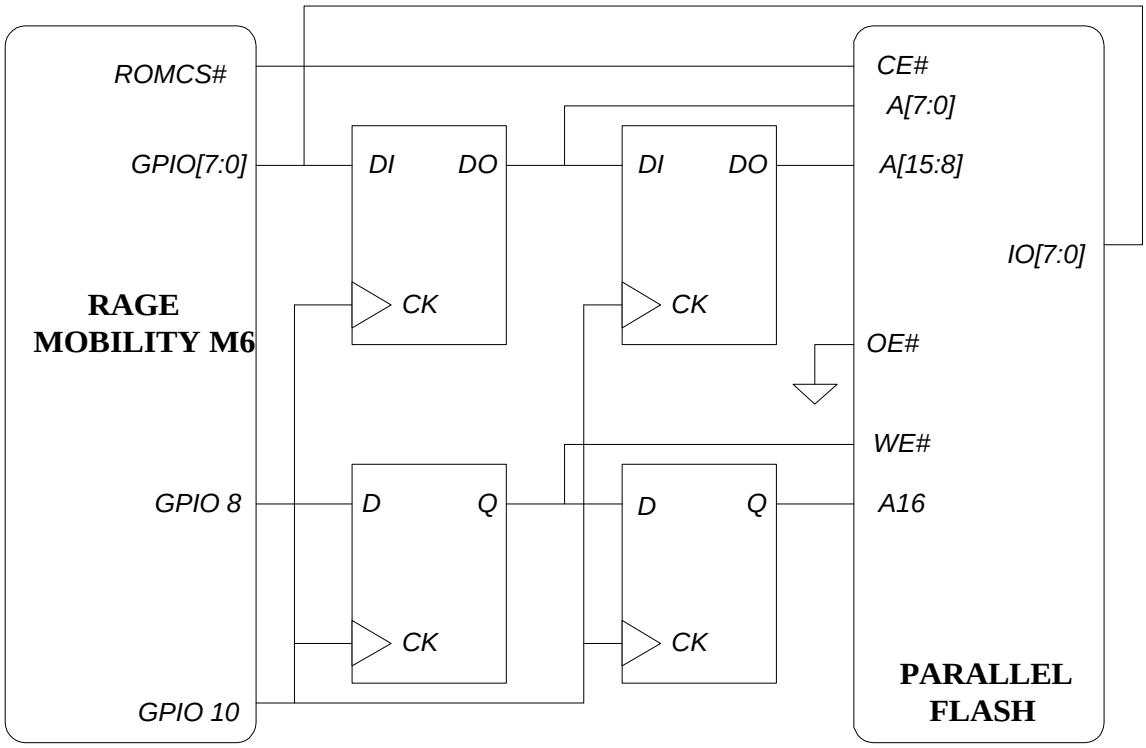


Figure 28*: *BIOS Interface – Parallel EEPROM Configuration

7.2.3 ROM Chip Select - ROMCS#

For motherboard designs, do not connect GPIO[13:11]. Those pins have internal pull-downs. This will prevent BIOS cycles from occurring. If those pins are not strapped properly, it might incorrectly trigger BIOS cycles and result in the failure of the system to boot up the video.

7.2.4 EEPROM

To connect the address and data lines to these devices, follow the convention shown in the reference schematics. Since there can be significant loading on the Address bus, use an optimized layout to keep traces as short as possible. The EEPROM can be either 2.5V or 3.3V device (5V signaling is not supported). To ensure its reliable operation, install decoupling capacitors between their VDDC and ground pins as shown in the reference design schematics.

7.2.5 Straps on the GPIO lines

The straps that are implemented on the GPIO lines must be connected to a discrete tristate-able buffer. This buffer is enabled during RESET, at which time the straps are read and latched into the controller. If a buffer is not used, improper latching of these straps can occur. This is because the devices on the GPIO interface may not properly tristate the GPIO lines during RESET. If GPIO lines are not used

for anything else, a buffer is not required. The ‘1’ sense on the straps on the GPIO lines is set with pull-up resistors to 3.3V. The ‘0’ sense is set with pull-down resistors to ground. The following figure shows this kind of implementation.

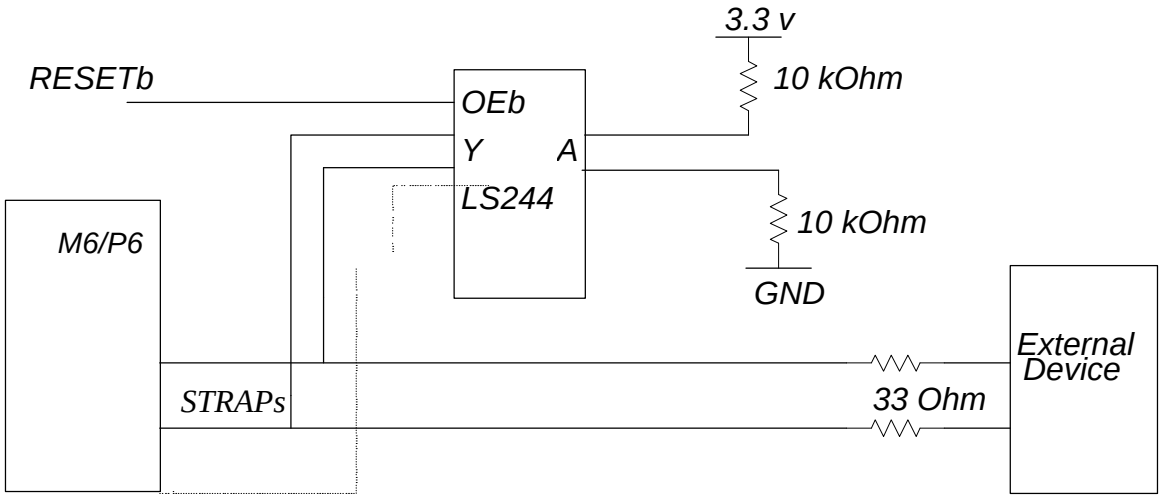


Figure 29 Straps Implementation

8 Crystal Oscillator and Clock Pins (XTALIN and XTALOUT)

The oscillator pins can be used with an external crystal network or an externally generated CMOS compatible clock source. The oscillator consists of a large inverter with an internal disable signal (EN), which disables the oscillator.

8.1 Mode 1: External CMOS-Compatible Clock Input

This mode supports a non-inverting input and an inverting input for buffer output pin OUT.

If the internal disable signal EN is set to logic zero, the inverter is off and its output is connected to a 10k resistor. The pin XTALIN is normally left unterminated when using an external CMOS-compatible clock input to the pin XTALOUT. The input clock is buffered into the chips.

If the internal disable signal EN is set to logic high, the pin XTALOUT is normally left unterminated when using an external CMOS-compatible clock input to the XTALIN pin. The input clock is inversely buffered into the chips. However, a 10 k-100 k load resistor to ground may be used to reduce generated radio frequency interference (RFI) noise emission.

8.2 Mode 2: Crystal Oscillator

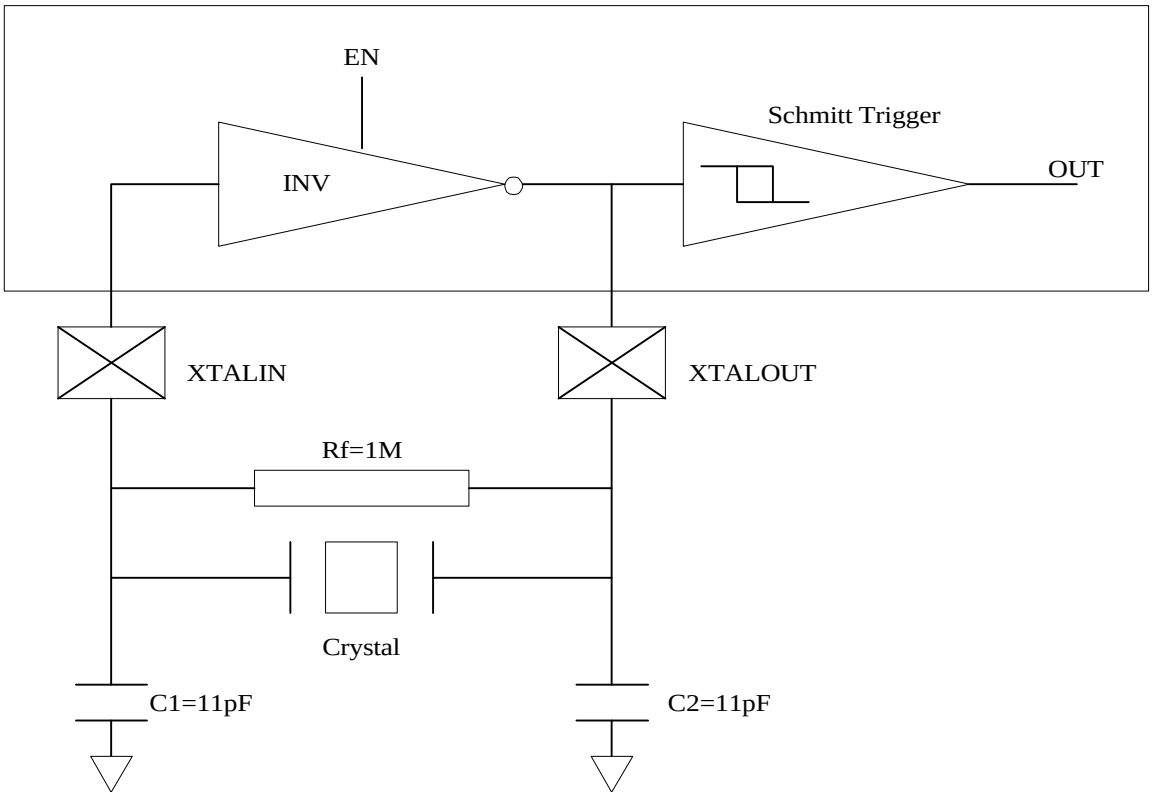


Figure 30: Oscillator Circuit

Figure 30: Oscillator Circuit shows the internal and external components of a crystal oscillator, (called the Pierce oscillator, also known as a parallel resonant crystal oscillator). The crystal oscillator works at 27.000Mhz. The resistor Rf provides a direct current bias to the input so that the inverter operates in its linear region as an inverting amplifier. The inverting amplifier supplies voltage gain and a 180-degree phase shift. The crystal combined with C1 and C2 form a tuned network that stabilizes the frequency and supplies another 180-degree phase shift feedback path. In steady state, this circuit has an overall loop gain equal to 1 and an overall phase shift equal to 0. To ensure that oscillations will start, the closed loop gain must be greater than 1, while at the same time the voltage at XTALOUT is growing over multiple cycles. The voltage increases until the inverter amplifier saturates.

The values of external components are dependent on IC processing technology, printed circuit board capacitance and inductance, socket capacitance, operating voltage, crystal technology, and frequency. Typical values are as follows:

Rf = 1M – 20M (higher values are sensitive to humidity; lower values reduce gain and could prevent startup)

Cl = 5pF – 21pF (value is usually fixed)

C2 = 5pF – 21pF (value is usually fixed, but may be varied to trim frequency)

8.3 Application Notes

The oscillator circuit is inherently a very high-impedance, closed-loop feedback system. When a standard oscilloscope probe is connected into the circuit, additional capacitance and resistors are added in the circuit, which will usually affect oscillator performance. An active FET probe with input capacitance below 2pF and input resistance above 5M could be used to monitor the circuit.

PCB traces of the oscillator layout should be kept as short as possible. The pins XTALIN and XTALOUT should be isolated from each other and adjacent circuitry by routing ground paths. Parasitic capacitance at the pins is just added in parallel with C1 and C2.

9 Analog Display

9.1 Block Diagram

The analog display section includes the signals that drive the display monitor and the signals dedicated to the operation of the internal DAC, as shown in the following figure.

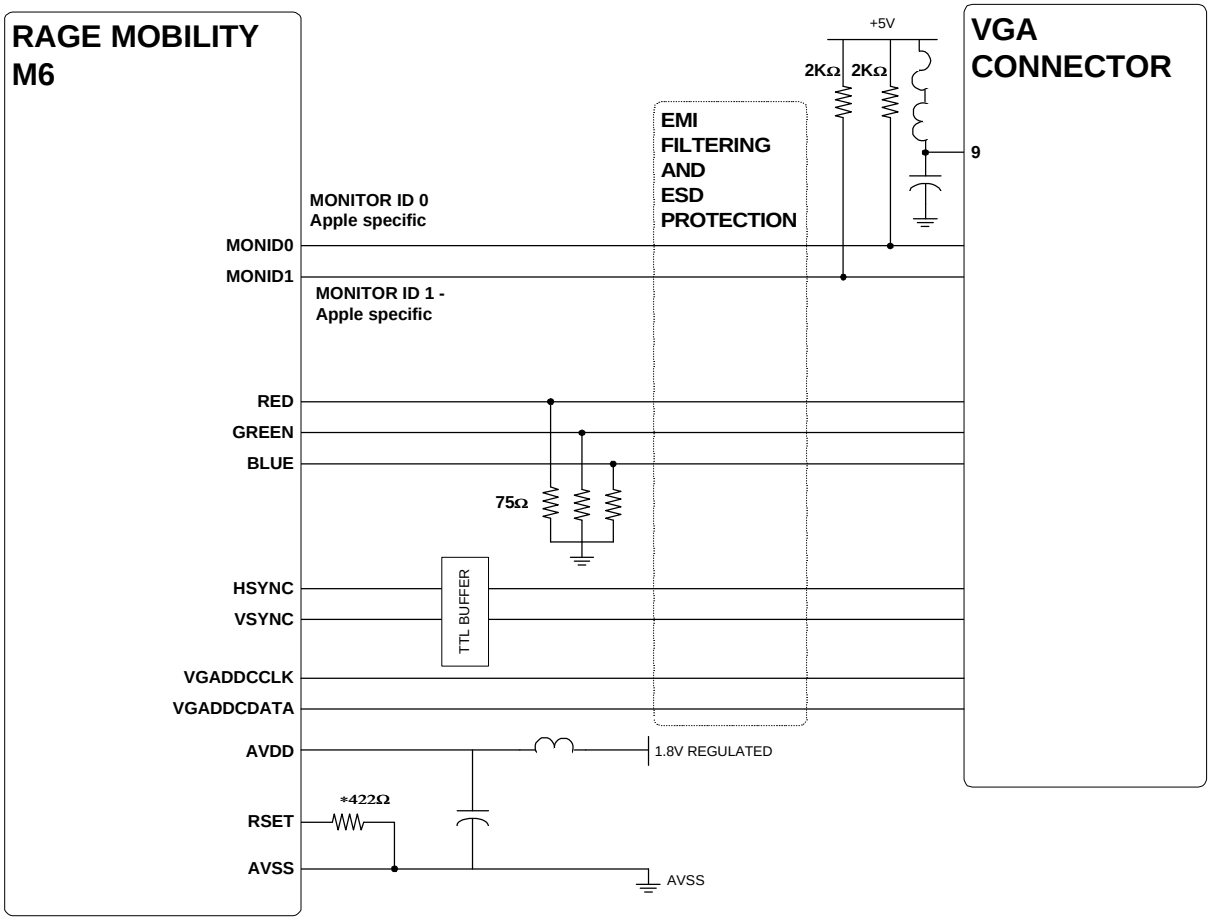


Figure 31: Analog Display Section

9.2 CRT Interface

9.2.1 Filtering

The goal is to achieve the best display quality while keeping the emissions of radio frequencies within the standards set by various regulatory agencies. Typically, the goal is to achieve compliance with the following standards: FCC/C.I.S.P.R. Class B, Canadian ICES-003 Class B, CE Directives 93/68/EEC and 89/336/EEC, and Australian ACA.

Use bypass capacitors and ferrite beads (configured in a π scheme) on all interface lines. Select values for the filtering components to provide sufficient filtering to meet the emission requirements while maintaining the quality of the video signal. The recommended values for these components are shown in the reference design schematics. However, values may vary for your specific design. The degree of variance depends on the ability of the motherboard or system enclosure to suppress or contain emissions.

Excessive filtering of the RGB signals can result in poor image quality. An attempt to compensate for a monitor that does not have adequate EMI suppression capability may result in excessive filtering.

9.2.2 ESD Protection

Large transient voltages may enter from the connector when certain monitor types are attached to the design. The RAGE MOBILITY M6 I/O buffers provide sufficient ESD protection to prevent controller damage from such transients. However, to add an additional margin, install surge-protection (i.e. clamping) diodes on the R, G, B, MONID, VSYNC#, and HSYNC# lines. The use of these diodes is recommended, but not mandatory.

9.2.3 RGB Termination

Analog DAC outputs (Red, Green, and Blue) can drive a 37.5Ω equivalent load. To match the 75Ω impedance of the CRT, connect 75Ω pull-down resistors (in parallel with the CRT) on these lines.

It is important to keep the impedance of the RGB lines as close as possible to the ideal 75Ω. Impedance mismatch between the RGB lines and the CRT may result in excessive reflections on these lines. If the amplitude of the reflections is too large, it will cause image ghosting.

9.2.4 Horizontal and Vertical Syncs

HSYNC and VSYNC are TTL outputs that offer programmable polarity to the display monitor. To add fanout drive, install CMOS buffers. CMOS buffers are preferred because of symmetrical drive and higher levels. The added drive will eliminate potential ‘no video’ problems. Insufficient drive on the HSYNC and VSYNC lines can be a problem with low core-voltage controllers.

To dampen the effect of reflections, both HSYNC and VSYNC must be source-terminated with series resistors. Place these resistors as close as possible to the VGA connector.

Care should be taken not to over filter HSYNC. Excessive rise and fall times on this signal can cause pixel jitter.

9.2.5 DDC Interface

The RAGE MOBILITY M6 controllers dedicate two I/O pins to the DDC interface (i.e. VGADDCDATA and VGADDCCLK). They are all used to implement DDC1 and DDC2B support. To maintain sufficient TTL levels on these signals, install pull-ups to the +5V rail after the FET that is added to protect inputs from the signal level bigger than 3.3V (please look at reference schematic for more details).

To dampen the effect of reflections, install series resistors (source termination) on the DDC and MONID lines. Place these resistors as close as possible to the VGA connector.

9.2.6 VGA Connector

Use the industry standard 15-pin D-type female connector or its Blue variant. If the Blue connector is used, connect pin 9 to the +5V rail and protect it by installing a 750mA self-resetting fuse. To reduce transient noise on this pin, connect a decoupling capacitor and a ferrite bead as shown.

9.3 DAC Interface

This interface is dedicated to the operation of the internal DAC. It consists of the RSET, AVDD, and AVSS pins. Inadequate decoupling, improper grounding, or an incorrect value for the RSET resistor on these pins can compromise image quality.

9.3.1 AVDD and A2VDD

These are the dedicated power pins used exclusively for the internal DACs. These pins require a clean power source to avoid noise injection into the DAC. Noise on the power line can cause pixel jitter on the display monitor.

Connect AVDD and A2VDD directly to the AVDD and A2VDD regulator via a ferrite bead. Connect decoupling capacitors between this pin and AVSS, A2VSS ground. Place the capacitors as close as possible to the power pin. To keep trace impedance low, the width of the power trace from the regulator to the controller should be greater than 15mils. The length of the trace is less than 2.5 inches.

9.3.2 AVSS and A2VSS

There are four AVSS pins on the RAGE MOBILITY M6 controller. Two are dedicated for grounding for the DACs. The other two are dedicated for grounding the DAC Band Gap Reference. To keep these pins bounce free, install decoupling capacitors between these and power.

9.3.3 RSET and R2SET

To set the full-scale DAC current, connect a high-precision (i.e. 1% tolerance) resistor connected between the RSET pin and the AVSS ground pins. The value of this resistor determines the 'white' voltage level of the RGB outputs. A smaller value of RSET corresponds to a higher voltage level and thus a brighter CRT display. The target value of this level is 700mV. For the most up-to-date RSET values, please contact ATI's field application engineers.

10 Digital Flat Panel Interface

10.1 Overview

The digital flat panel interface allows the connection of digital flat panels. The RAGE MOBILITY M6 offers digital flat panel support. The RAGE MOBILITY M6 controller provides digital flat panel support through an integrated TMDS (Transition Minimized Differential Signaling) and integrated LVDS (Low Voltage Differential Signaling). For the RAGE MOBILITY M6 controller, a digital flat panel can be connected directly, through the clock and RGB differential pairs.

For the RAGE MOBILITY M6 controllers, digital flat panel support is provided through an integrated TMDS and an integrated LVDS. These display engines allow for different timings and resolutions for concurrently operating digital flat panels and CRTs.

10.2 Integrated LVDS interface

The RAGE MOBILITY M6 controller uses an integrated LVDS transmitter. The integration of this feature helps to reduce component pinout counts, simplifies the interface, and increases operational reliability.

10.2.1 Data and Clock Analog Differential Pairs - TXOUT and TXCLK

Ten analog differential pairs make up the LVDS connector's data and clock signals. Eight pairs are dedicated for the RGB data and two pairs are dedicated for the clocks.

AC coupling for these signals is optional. However, if AC coupling is used, place the coupling components as close as possible to the DFP connector. For the proper configuration and values, refer to the reference design schematics. For more details regarding the layout of these differential signals, read the subsection at the end of this chapter.

10.2.2 Power and Grounds Pins – LPVDD, LPVSS, LVDDR, LVSSR

Power for the internal LVDS transmitter is provided through the LVDDR and LPVDD pins. LVDDR supplies power to the LVDS macro and LPVDD supplies its dedicated PLL.

LVSSR and LPVSS are the corresponding ground pins.

Install series ferrite beads on the power pins to block out the noise from the power supply. Install decoupling capacitors between LVDDR and LVSSR, and between LPVDD and LPVSS. Place the capacitors as close a possible to the power pads. For more details regarding the configuration of the decoupling circuits, refer to the reference design schematics.

Always provide power and grounding for the integrated LVDS transmitter.

10.2.3 Unused Pins

Depending on the type of controller package, several DFP pins may remain unconnected. Unless otherwise noted, unused pins may remain unconnected.

10.3 Integrated TMDS interface

The RAGE MOBILITY M6 uses an integrated TMDS transmitter. This offers the advantages of reduced component and pinout counts, simplified interface, and increased operational reliability. Some basic knowledge of high-speed board design and differential signal theory is required.

TMDS (Transition Minimized Differential Signaling) is a way to communicate data using two wires with opposite current/voltage swings. It offers the advantage of low power and low noise transmission.

10.3.1 PCB Layout

For a successful implementation of a TMDS interface, observe the following guidelines for PCB layout.

10.3.1.1 Placement of Components

Keep the differential lines short. Place the TMDS connector as near as possible to the controller's integrated TMDS output pins.

Install bypass capacitors at the TMDS transmitter's power pins. For best performance, place the tantalum surface-mount capacitors close to power and ground pins.

Place the clock source (OSC or XTAL) as far away as possible from the TMDS transmitter.

10.3.1.2 Routing TMDS Lines

To maximize differential benefit, keep differential pairs parallel and close to each other, and maintain identical physical and electrical length.

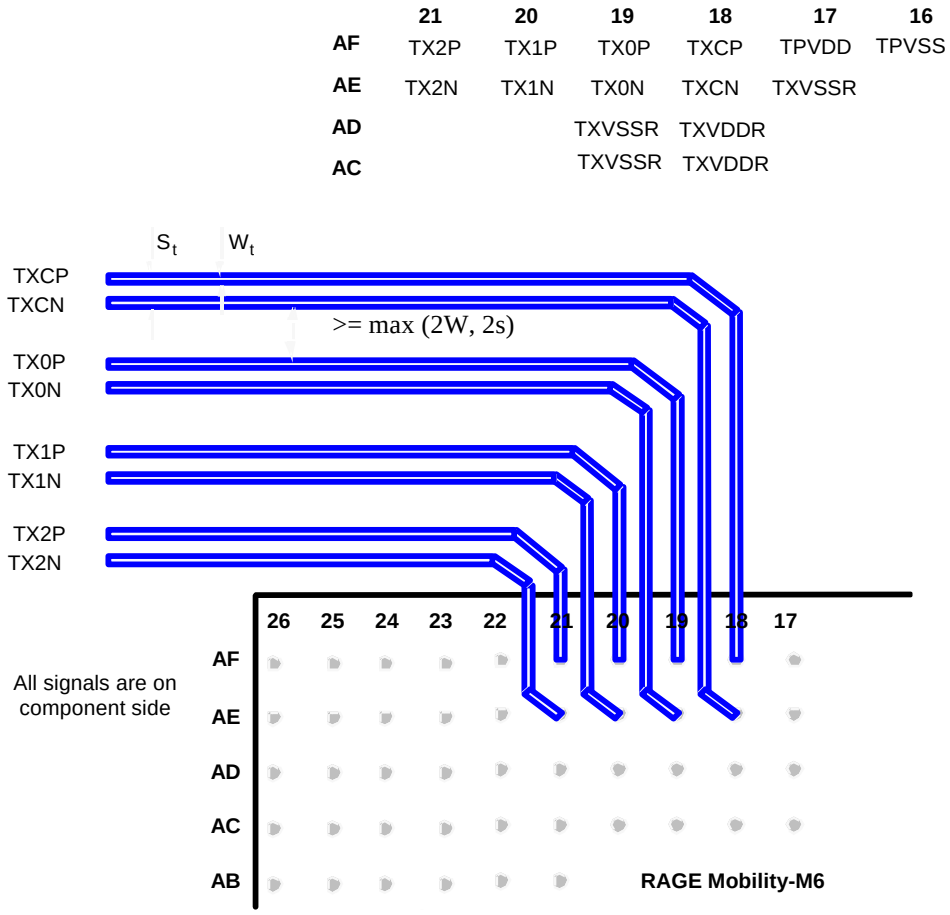


Figure 32: Routing TMDS Lines

To minimize cross talk, keep large distances between the TTL/CMOS and TMDS signals.

Use multiple vias to connect to power and ground, traces, and planes. Make all power and ground traces short and wide.

Use a ground-current return path that is short in length. Place this path between the driver and the connector. The best current return path is a uniform, unbroken ground plane.

To reduce the skew within the pair, avoid unbalanced layer change and pair spacing.

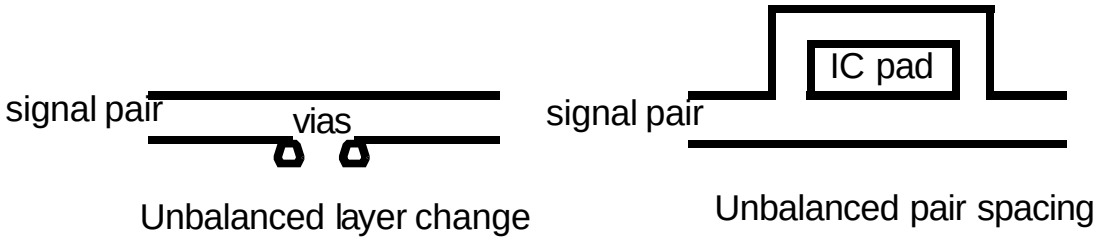


Figure 33: Avoid Unbalanced Layer Change

Place a test point on the trace line.

Figure 34: A Test Point

10.3.1.3 Impedance Considerations

Impedance matching is very important even for short runs in TMDS design. Ensure proper impedance matching of PCB trace to avoid reflections. If impedance matching problems occur, adjust the value of the impedance matching resistor on the TMDS receiver side.

When routing TMDS pairs, minimize the number of vias to avoid impedance discontinuity.

Use rounded (i.e. avoid sharp 90 degree) edges to reduce change in impedance, especially critical at high frequencies.

10.3.1.4 Using Shields to Guard Against EMI and Cross talk

According to recommendations from “DFP TMDS Differential Trace Layout Configuration”, the differential trace length from the TMDS transmitter to the connector should be kept equal or less than 1.0 inch. This reduces the transmission line characteristics of the board trace (trace width and spacing) to be of a second order effect (i.e., less critical).

However, when longer traces are unavoidable, special attention must be paid to increased possibility of cross talk from adjacent TMDS signal pairs and from non-TMDS related digital switching activities. In such cases, the following are

recommended:

- Use cable shielding to reduce EMI. Shields should be connected directly to both the driver enclosure and the receiver enclosure whenever possible.
- To reduce cross talk between adjacent TMDS pairs, keep the distance(W) at least twice as large as the spacing within a pair .

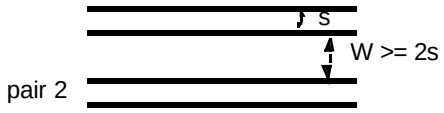


Figure 35: Avoiding Cross talk

- When cross talk is unacceptable, use guards traces. The following figure shows the recommended layout design using guard traces.

Note: A shield must not be placed between the traces of a differential pair.

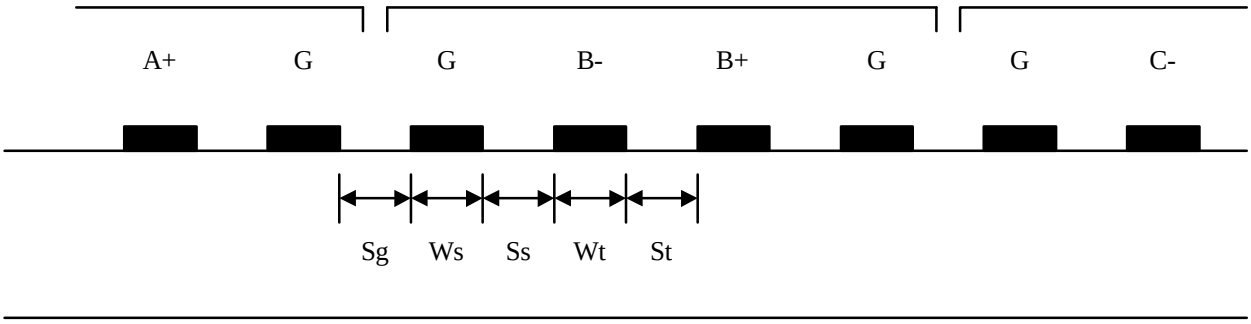


Figure 36: Guarded Differential Pair

10.3.1.5 Power Source Cleanliness

Make sure the power supplied to the transmitter is clean. Irregular power source may cause clock jitters and a noisy screen on the panel.

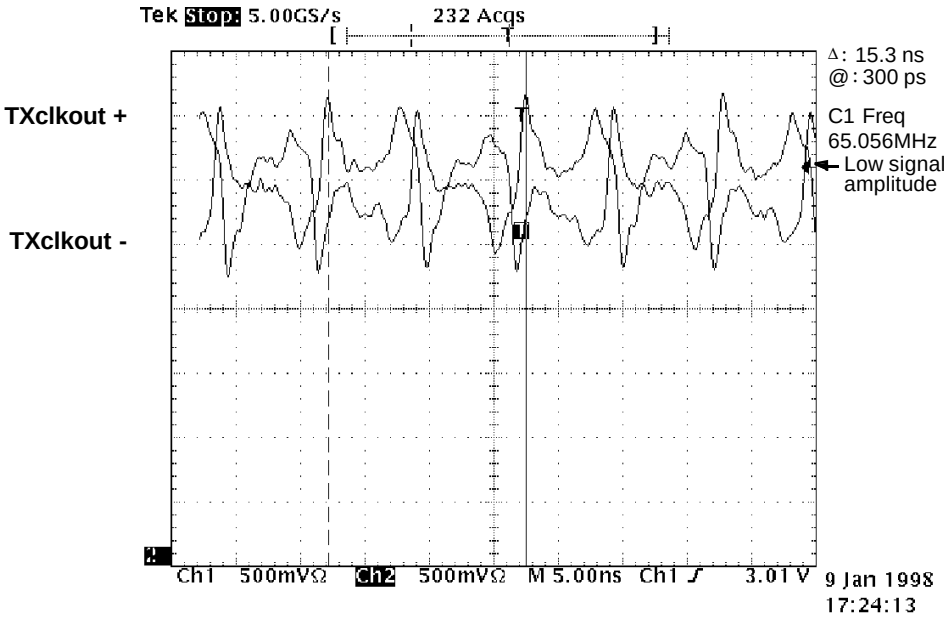


Figure 37: Waveform polluted by Unstable Power

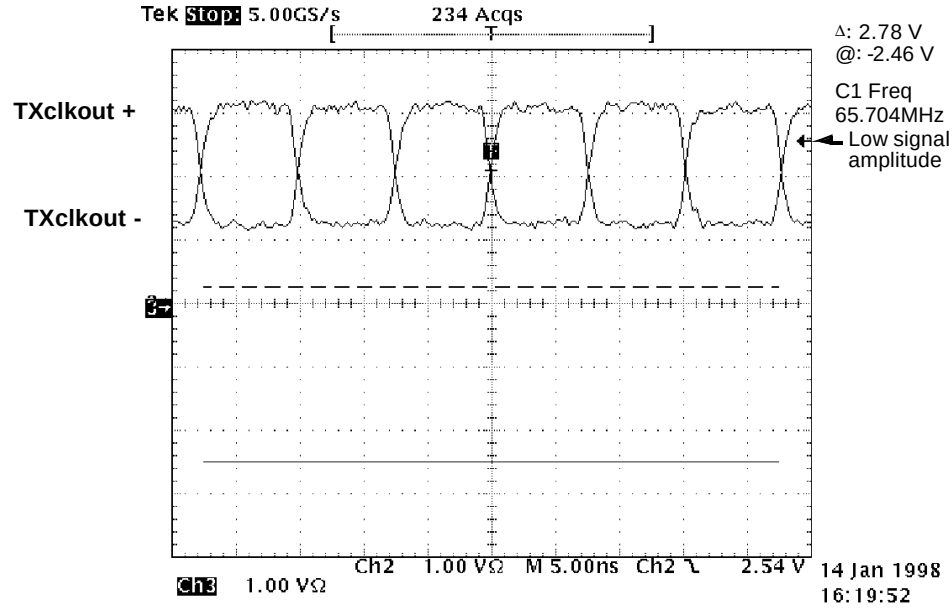


Figure 38: Clear TXCLK Output

10.3.1.6 Trace Parameter Calculations

The following shows how intra-pair spacing (s) and trace width (W) can be determined while staying close to the VESA stipulated transmission line characteristics of Zdiff = 100W, Zo = 50W.

Two methods can be used: the TMDS Calculator from the document “DFP

Board Layout Guidelines" (obtainable through www.vesa.org), or a numerical technique.

10.3.1.7 Using the DFP TMDS Calculator

The DFP TMDS Calculator equations (see DFP Board Layout Guidelines Rev 2, page 1) provide a relatively simple method for determining optimal intra-pair spacing and trace width to achieve a good board-to-cable matching. Normally, when the cross talk between differentially driven pair of signal lines (i.e. signal bundles) are minimized (by following certain rules of thumb for spacing between the bundles), the calculated results using the Calculator are in very good agreement with those generated by a numerical method such as the "numerical field solver".

When using the Calculator, the following relations must be borne in mind:

$$Zdiff \propto (s/W)$$

Equation 2: Zdiff

$$Zo \propto (1/W)$$

Equation 3: Zo and W

Where the symbol $\propto$ means "is proportional to".

$$\text{If } Zdiff > 1.9\ Zo\text{, let } Zdiff = 1.9\ Zo$$

Equation 4: Zdiff and Zo

Equation 4 is derived from the observation that when Zdiff is larger than or equal to twice Zo, the value of s increases rapidly. Limiting the ratio to 1.9 allows reasonable trace spacing s to be used.

The Calculator is designed with Zdiff as a hard constraint or constant. Applying this to Equation 2 means that as s is increased, W must also be increased to keep Zdiff constant. This results in:

$$W \propto s$$

Equation 5: W and s

Combining Equation 5 and Equation 3 results in Equation 6. This means that an increase in s causes a decrease in Zo.

$$Zo \propto (1/s)$$

Equation 6: Zo and s

The Calculator can be used in two ways:

- Method 1: Fix Zdiff and feed in s, calculate Zo and W
- Method 2: Feed in s and W, calculate Zdiff and Zo

The following two tables give examples of two such calculations.

Table 18: Method 1 - Fix Zdiff and feed in s and calculate Zo and W

Constants:	**Er**	= 4.2	Dielectric constant (FR-4 at 1GHz)
	To	= 0.7 mil	Outer trace thickness
	Ti	= 1.4 mil	Inner trace thickness
	h	= 4.3 mil	Height of outer layer
	Zdiff	= 100 Ω	Differential impedance
Input:	**s**	= 12 mil	Minimum trace spacing
Output:	**Zo**	= 51.70315 Ω	Characteristic impedance
	W	= 6.517332 mil	Trace width

Conversion factor: 1 mil = 0.001 inch, i.e. 1 mm = 39.37 mil or 1 mil = 0.0254 mm.

Table 19: Method 2 - Feed in s and W and calculate Zdiff and Zo

Constants:	**Er**	= 4.2	Dielectric constant (FR-4 at 1GHz)
	To	= 0.7 mil	Outer trace thickness
	Ti	= 1.4 mil	Inner trace thickness
	h	= 4.3 mil	Height of outer layer
Input:	**s**	= 10 mil	Minimum trace spacing
	W	= 7 mil	Trace width
Output:	**Zo**	= 49.47561Ω	Characteristic impedance (only a function of W, not of s)
	Zdiff	= 93.85704 Ω	Differential impedance (adjust s for nearest value)

To illustrate the use of the Calculator, let us attempt the design target of Zo = 50Ω and Zdiff = 100Ω. It will be seen that there is a trade-off between the area or pitch (sum of s and W) and meeting the targets. We start with Calculator 2, and the

consideration of Equation 4, according to which Zdiff should be no larger than 1.9 times Zo. Let's therefore set Zdiff to 95Ω (Zdiff = 1.90*Zo = 1.90*50 = 95). Using this value, s is calculated to be about 12mil.

We now use Calculator 1 to trade off "meeting target Zo" with "meeting target Zdiff". By setting s to the calculated value of 12 mil, the other design parameter W is now calculated. Its value will be larger than the original 7mil given in Table 18: Method 1 - Fix Zdiff and feed in s and calculate Zo and W, the value of Zo will also be different from the targeted 50Ω. Now, by varying only s, we can build up a spreadsheet using "what-if scenarios", from which reasonable values for W and Zo can be picked.

10.3.1.8 Using Numerical Analysis

In situations where trace guards are implemented (Figure 36: Guarded Differential Pair), the calculations for deriving correct trace spacing and trace width can be complicated. In fact, a significant error will result for Zdiff and Zo values if they are derived from the TMDS Calculator equations. For correct calculations, numerical technique is required.

The following trace parameters calculated using a numerical technique are recommended for Er = 4.2, h = 4.3 mil, and To = 0.7 mil:

Signal Trace widths (Wt): 7 mil
Signal spacing (St): 7 mil
Shield width (Ws): 7 mil
Shield to signal spacing (Ss): 7 mil
Shield to Shield spacing (Sg): 7 mil

10.3.1.9 Sample Trace Parameter Calculations for Different Boards

Trace width and corresponding Zdiff and Zo on several add-in boards were evaluated. The results are summarized in the following table.

Table 20: Example Differential Pair Trace Calculations

Board ID	Er mill	To mill	Ti mill	H mill	S mil	Zdiff Ω	Zo Ω	W mill
Layout design, using the numerical method	4.2	0.7	1.4	4.3	7	92.54	51.44451	7.88
55300-00B, using DFP Calculator	4.2	0.7	1.4	8	10	100	58.45036	12.36
56400-00B and 56500-00A, using DFP Calculator	4.2	0.7	1.4	8	6	100	65.24358	10.08
56300-00A, using DFP Calculator	4.2	0.7	1.4	8	5	100	67.88217	9.38

Board ID	Er	To	Ti	H	S	Zdiff	Zo	W
	mill	mill	mill	mill	mil	Ω	Ω	mill

Er Dielectric constant (FR-4 at 1GHz)
To Outer trace thickness
Ti Inner trace thickness
h Height of outer layer
s Minimum trace spacing
Zdiff Differential impedance
Zo Characteristic impedance
W Trace width

10.3.2 Data and Clock Analog Differential Pairs - TX and TXC

The data and clock to the TMDS connector consists of four analog differential pairs. Three pairs are dedicated to the RGB data and one is dedicated to the clock. AC coupling on these signals is optional. However, if coupling is used, place the coupling components as close as possible to the DFP connector. For more details regarding the configuration of and values for the AC coupling circuit, refer to the reference design schematics. For more details regarding the layout of these signals, refer to the remaining subsection at the end of this chapter.

10.3.3 Hot Plug Detect - HPD

Hot plug detect is one of the three signals used to implement the VESA Plug-and-Play Hot-Plugging scheme. The other two are the DDC clock and the DDC data signals. This scheme protects the display from harmful conditions that are created when receiving the data at the incorrect frequency or format. The hot plug detect line is also called the charge power line. When a display is connected, voltage on this line will rise to over 2V (it may even increase to 20V). A detection circuit inside the RAGE MOBILITY M6 controller uses this voltage as indication that the display is ready and waiting for the internal TMDS to be enabled. Because the charge on this line can increase to 20V, install a clamping circuit to prevent damage to the input pin. This circuit consists of a 2.5V zener diode and a shunt resistor. Install a series resistor to protect against surge current and maintain the voltage level on the display side. For circuit details, refer to the reference design schematics.

10.3.4 DDC Clock and DDC Data – DVIDDCCLK and DVIDDCDATA

These signals are used to implement the VESA DDC2B protocol and the PnP Hot-Plugging scheme. To maintain robust TTL levels on these signals, install pull-up resistors to the +5V rail after the FET transistors that protect inputs from signals that have higher level than 3.3V (for more details please refer to the reference schematic).

10.3.5 Power and Ground Pins – TPVDD, TXVDDR, TPVSS, TXVSSR

Power for the internal TMDS is provided through the TXVDDR and TPVDD pins. TXVDDR supplies power to the TMDS macro and TPVDD supplies power to its dedicated PLL. TXVSSR and TPVSS are the corresponding ground pins.

Install series ferrite beads on the power pins to block out power supply noise. Install decoupling capacitors between TXVDDR and TXVSSR, and between TPVDD

and TPVSS. Place the capacitors as close as possible to the power pads. For more details regarding the configuration of the decoupling circuits, refer to the reference design schematics. Always provide power and grounding for the integrated TMDS (regardless of whether a DFP is used).

10.3.6 Unused Pins

Depending on the controller package, several DFP interface pins remain unconnected. Unless otherwise noted, unused pins remain unconnected.

10.4 Layout Guidelines for Differential Signals

Use these layout guidelines for differential signals for all RAGE MOBILITY M6 designs that use digital flat panel displays. These layout considerations are similar to other graphics controllers that use a digital flat panel interface. This section includes important excerpts from the design guides of such controllers.

10.4.1 Suppression of Common-Mode Noise

Differential noise on balanced pairs is usually not a problem. Common-mode noise is generated by currents of the same polarity flowing along both of the signal lines simultaneously. Common-mode noise is a major concern for differential signal lines, because even a very low value of common-mode current may cause very high emissions. Inductors can be used to suppress common-mode currents. Place these inductors near the connector where the differential signals connect to the cable. Common-mode inductors are not shown in the reference design schematics because their values and use are application specific.

10.4.2 Layout Considerations

Observe the following guidelines when laying out differential signals:

- Keep differential pairs parallel and close to each other. Maintain identical physical and electrical lengths.
- Keep the differential lines short, or place the controller close to the digital flat panel connector.
- Avoid sharp angle turns when routing differential traces. This will keep impedance low during high-frequency operation.
- Separate the TTL/CMOS signals from differential signals to avoid cross talk. To increase distance, run ground trace or use differential plane between TTL/CMOS and differential signals.
- Use a ground plane between differential signal pairs on connector and cable.
- Ensure proper impedance matching of PCB traces to avoid reflections.
- Place all termination resistors as close to the receiver as possible.

10.4.3 Trace Routing

Ensure that the lengths of both lines of each differential pair are equal. It is preferable to route all differential signals on the same side as the transmitter and connector to avoid the use of vias (this is possible for the through-hole MDR20 connector, but not for the SMT variant). When balancing intra-pair traces, it is important to ensure that any introduced discontinuities are equal to both members of the pair. Intra-pair skew should be less than 0.100 inches.

10.4.4 Trace Shielding

If board space permits, trace shields are useful for EMI suppression. Shields should be added on the same layer as the differential traces, between and surrounding the signal pairs. The shield traces must be connected to the AGND plane directly beneath them, using vias placed every 0.5 inches along their path. Terminations to the AGND plane should be placed on both sides of the trace, and there should be no dangling guard traces.

A good connection to AGND is important to keep the high-speed currents from escaping into other circuits. TTL signals and other noise sources should be distanced from the differential pairs to eliminate cross-coupling, although use of trace shields helps reduce the possibility of this from occurring. The shields must be distanced at least twice the differential trace width or separation (whichever is greater) from the differential pair. If guard traces are not used, it is recommended that pair to pair spacing be greater than 2 to 3 times the intra-pair spacing.

10.5 TV Out Interface

10.5.1 Component Placement

Place the controller as close as possible to the output connectors in order to minimize noise pickup and reflections due to impedance mismatch. Place discrete components as close as possible to the associated controller pins. Avoid using vias as much as possible.

10.5.2 Ground Plane

A common digital and analog ground plane is recommended.

10.5.3 Power Plane

Separate digital and analog power plane is recommended. Connect these two lanes at a single point through a ferrite bead.

10.5.4 Device Decoupling

Place all decoupling capacitors as close as possible to the controller. Surface mount capacitors are recommended for minimum lead inductance. Keep the trace length between groups of power and ground as short as possible to minimize inductive ringing.

10.5.5 Power Supply Decoupling

The pair of decoupling capacitors (22μF and 0.1μF) is used on each group of power and ground. Place these capacitors as close as possible to the associated controller pins and connect them with short wide traces. The 22μF capacitors are used to filter the low frequency ripple from the power supply. The 0.1μF capacitors are used to reject high-frequency noise from the power supply.

10.5.6 Digital Signals Interconnect

Isolate the digital inputs to the controller as much as possible from the analog outputs and other analog circuitry. These input signals should not overlay the analog power plane or analog output signals.

10.5.7 Analog Signal Interconnects

Avoid routing digital traces under or adjacent to the analog output traces to avoid cross talk from the digital lines. Avoid overlaying the video output signals on the analog power plane to maximize high frequency power supply rejection. Place the load resistor as close to the controller as possible to minimize reflection.

10.6 External TMDS interface

10.6.1 Component Placement, ground and power planes

Place the external TMDS transmitter as close as possible to the graphics controller. Place discrete components as close as possible to the associated controller pins. Avoid using vias as much as possible. A common digital and analog ground plane is recommended. Separate digital and analog power plane is recommended. Connect these two lanes at a single point through a ferrite bead. Follow design rules and recommendations provided by TMDS transmitter manufacturer.

10.6.2 Digital Signals Interconnect

Isolate the digital outputs from the controller as much as possible from the analog outputs and other analog circuitry. These output signals should not overlay the analog power plane or analog output signals. Keep in mind that digital interface signals are running up to 165MHz frequency in case of 1600x1200 panel resolution. All digital interface signals to the external TMDS transmitter (except pixel clock) are flopped inside output buffer which provides minimum skew between signals at the output of the controller.

10.6.3 Analog Signal Interconnects

Avoid routing digital traces under or adjacent to the analog output traces to avoid cross talk from the digital lines. Avoid overlaying the video output signals on the

analog power plane to maximize high frequency power supply rejection. Place the load resistor as close to the controller as possible to minimize reflection. Follow the same rules that are explained in details in chapter 10.3 when routing traces from the output of external TMDS transmitter to the second DVI connector.

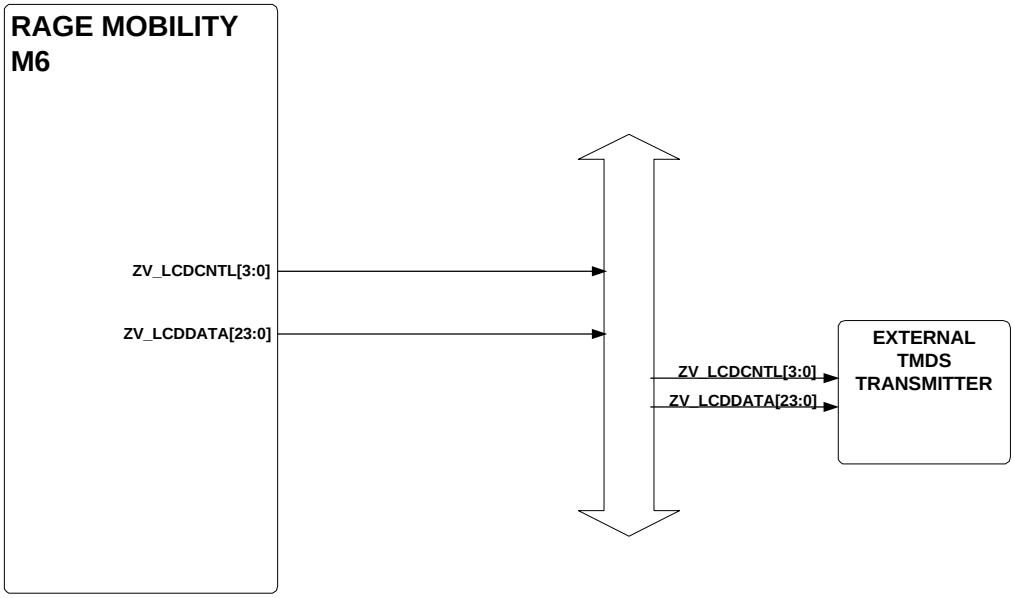


Figure 39: External TMDS support

11 ATI Multimedia Interface

A number of standard multimedia acronyms are used in the content of this chapter. The following is a list of the most common.

Table 21: Multimedia Channels

Channel	Description
DVS	Digital Video Stream
VIP	Video Interface Port
ZVPORT	Zoom Video Port

The multimedia interface allows the use of ATI products for multimedia applications. It supports a number of video protocols implemented through dedicated ports, namely DVS and Zoom Video. VIP interface is not supported with RAGE MOBILITY M6.

11.1 Overview

Depending on the supported multimedia devices that are attached, the RAGE MOBILITY M6 controller can dedicate up to 21 physical pins to the Multimedia interface. The assignment and configuration of these pins is carried out by the multimedia modules of the video BIOS and graphics drivers at initialization. The following figure shows the physical connections to the multimedia connector and to the multimedia companion chips that are included in ATI's reference designs.

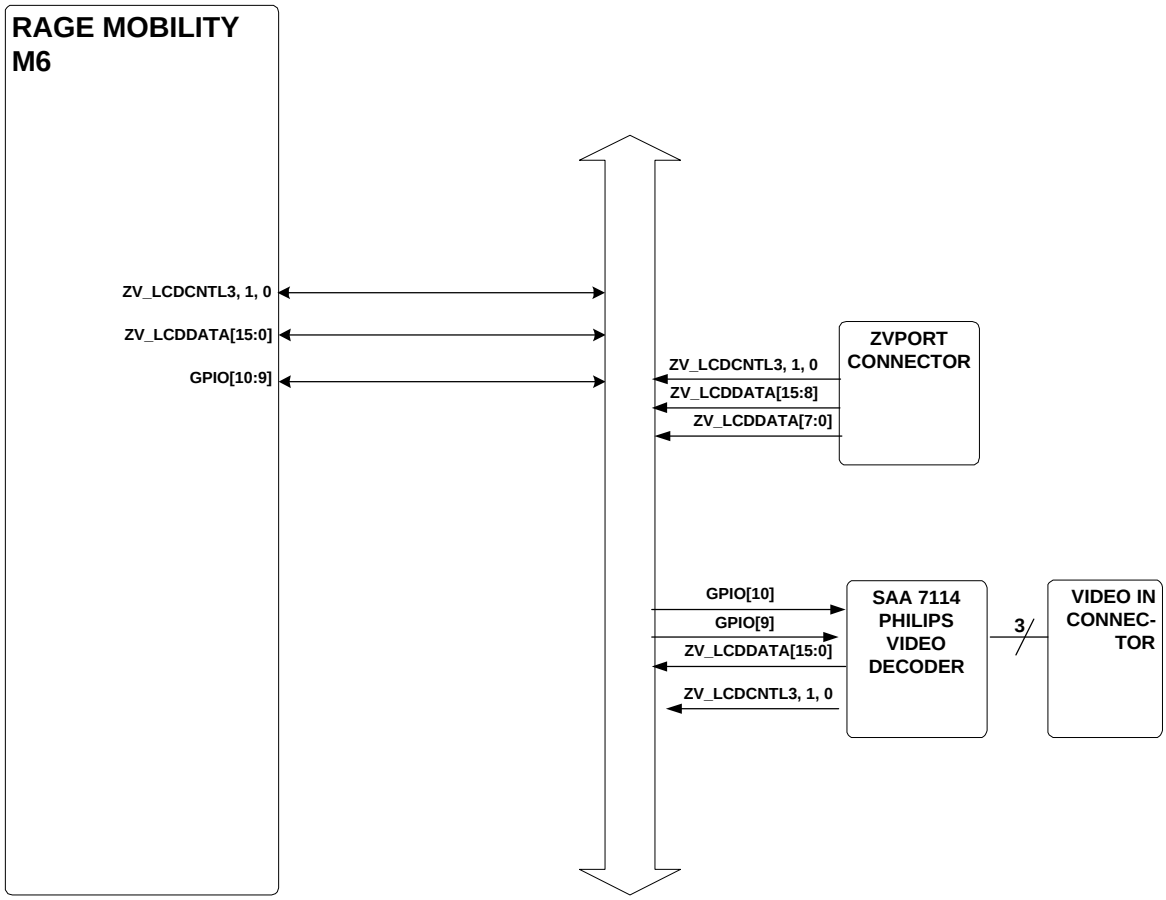


Figure 40: ATI Multimedia Interface

The following bulleted list shows a number of available design options. The decision on which option to implement is a tradeoff between requirements, costs and available real estate.

- RAGE MOBILITY M6 Controller + SA 7114 Philips Video Decoder + ZV Port Connector
- RAGE MOBILITY M6 Controller + ZV Port Connector

The same ZV_LCDDATA pins are shared between Multimedia Interface and external TMDS transmitter interface. Those two are mutually exclusive and cannot coexist at the same time. However, with proper multiplexing and providing signal that control the muxing, both interfaces can be implemented on the same design, but cannot be used at the same time.

Adherence to design guidelines for high-speed circuits is essential to the successful implementation of the multimedia interface.

The rest of the discussion in this chapter focuses on the individual ports that make up the multimedia interface.

11.2 DVS Port

This 8-bit DVS (Digital Video Stream) unidirectional port is used to input the digital video into the RAGE MOBILITY M6 controller. The video sources may be MPEG decoders or other video decoders such as Philips SAA7114. A wide range of video formats is supported, including CCIR565 and Zoom Video.

11.2.1 DVS Clock – ZV_LCDCNTL[3]

This is the pixel clock for the video-in stream.

11.2.2 DVS Data – ZV_LCDDATA[15:0]

Table 22: Video Port Pins Multiplexing

	ZV, Philips Port		Bt81975	
Signal name	**Pin name**	**Direction**	**Pin name**	**Direction**
ZV_LCDDATA(0)	Y0	I	YUV0	I
ZV_LCDDATA(1)	Y1	I	YUV1	I
ZV_LCDDATA(2)	Y2	I	YUV2	I
ZV_LCDDATA(3)	Y3	I	YUV3	I
ZV_LCDDATA(4)	Y4	I	YUV4	I
ZV_LCDDATA(5)	Y5	I	YUV5	I
ZV_LCDDATA(6)	Y6	I	YUV6	I
ZV_LCDDATA(7)	Y7	I	YUV7	I
ZV_LCDDATA(8)	UV0	I	ZVGPIO(0)	I/O
ZV_LCDDATA(9)	UV1	I	ZVGPIO(1)	I/O
ZV_LCDDATA(10)	UV2	I	ZVGPIO(2)	I/O
ZV_LCDDATA(11)	UV3	I	ZVGPIO(3)	I/O
ZV_LCDDATA(12)	UV4	I	ZVGPIO(4)	I/O
ZV_LCDDATA(13)	UV5	I	ZVGPIO(5)	I/O
ZV_LCDDATA(14)	UV6	I	ZVGPIO(6)	I/O
ZV_LCDDATA(15)	UV7	I	ZVGPIO(7)	I/O
ZV_LCDCNTL(1)	HREF	I	/	/
ZV_LCDCNTL(0)	VSYNC	I	/	/
ZV_LCDCNTL(3)	PCLK	I	PCLK	I

Note: In 8-bit video input mode, ZV_LCDDATA(17:8) could be used as general purpose I/Os.

11.2.3 Unused DVS Pins

All pins dedicated to DVS are internally pulled down. If the DVS ports are not used, the pins can remain unconnected.

11.3 Software I2C Bus

The I2C is the industry standard 2-bit serial bus used for programming multimedia devices such as video decoders, TV tuners, teletext decoders, and volume control. In RAGE MOBILTY M6, there is no HW I2C. However, two pins are

dedicated for SW I2C in order to facilitate software development.

11.3.1 I2C Data - GPIO[9]

This is the serial I2C data line.

11.3.2 I2C Clock - GPIO[10]

This is the I2C clock line.

12 Spread Spectrum Layout Guidelines

The RAGE MOBILITY M6 controller has support for external spread spectrum circuit (provisions are made for implementing different ones, namely the IMI SM530, the ICS MK1707A and the ICW W166). The following discusses the layout guidelines for IMI's SM530 case. Similar considerations apply when implementing the other two chips.

The SM530 spread-spectrum clock is a PLL-type hybrid circuit. This circuit contains both digital and analog circuits on the same die. To obtain the best possible performance, the phase detector, loop filter, and VCO are analog circuits that must operate in a very low-noise environment.

There are several ways to minimize this noise, such as placing bypass capacitors on all power pins and separating the analog and digital power and ground planes. The following diagram shows the first approach by placing the capacitors as close as possible to every power pin. In addition, all ground pins should be connected directly to the ground plane with little or no trace length.

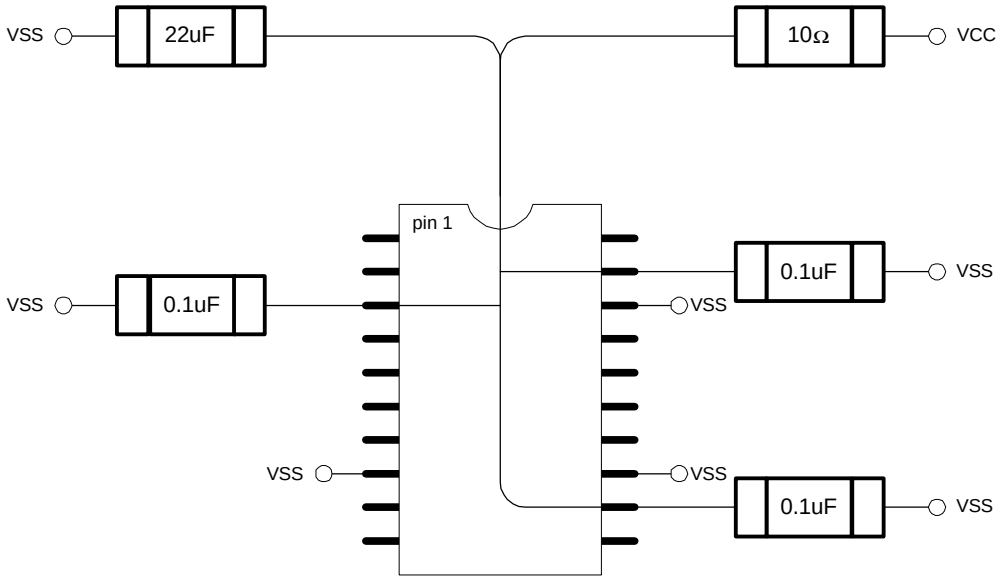


Figure 41: SM530 Single Power Plane Layout

Only the power and ground circuits of the SM530 have been shown. Other circuits such as the loop filter components must be located as close as possible to the loop filter pin (for best performance).

When powering the external spread spectrum chip do use a clean power supply. The operating voltage range of spread spectrum chips is from 3.3V to 5V but 3.3V is preferred in order to reduce power consumption. However, since many other

components in the laptops are powered by 3.3V, the supply is shared. Whenever components sink large currents from the 3.3V supply, like when accessing a HDD for example, the fluctuation in the power supply effects the output of the spread spectrum chip. This eventually causes corruption on the panel.

A 5V power supply is preferred to power the external spread spectrum chip. Using 5V increases noise margin and has been found to be effective in practice (we tested this on several OEM designs). If a 5V power supply solution is chosen then care should be taken at the signaling level. The Rage Mobility M6 chip is not 5V tolerant so an interface that translates the signaling level from 5V to 3.3V has to be implemented (for example, using FET transistors).

Adhering to the recommendations above will assure the success of the external spread spectrum chip implementation.

For complete details, refer to the reference design schematics.

13 Revision History

Date	Rev.	PDF	Description
Aug.22, 2000	0.1	DSG-216M6-00-01	Initial draft completed.
Aug 30, 2000	0.2	DSG-216M6-00-02	Added additional spread spectrum layout guidelines
Sept 1, 2000	0.3	DSG-216M6-00-03	Modified subsystem grounding; introduced specification about SSTL-2 interface for DDR memory, clarified terminations for HSYNC, VSYNC and DDC interface, replaced TTL buffers with CMOS buffers for HSYNC and VSYNC