Intel® 845MP/MZ Chipset Family Memory Controller Hub (MCH-M)

Specification Update

September 2002

Notice: The Intel® 845MP / Intel® 845MZ MCH-M may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number 251809-001

Contents

Revision History

Rev.	Draft/Changes	Date
001	Initial Release	September 2002

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel®845 Family Chipset-Mobile :82845MP/MZ Chipset Memory Controller Hub (MCH) Dataheet	250687-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the behavior of the Intel® 845MP / Intel® 845MZ chipset MCH-M to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® 845MP chipset MCH-M may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B-0	8086h	1A30h	04h

The Intel® 845MZ chipset MCH-M may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B-1	8086h	1A30h	05h

Caution

The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® 845MP chipset MCH-M may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B0	SL66J	RG82845MP	Production 82845MP MCH-M

The Intel® 845MZ chipset MCH-M may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B1	SL64T	RG82845MZ	Production 82845MZ MCH-M

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel 845MP chipset MCH-M steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Spcification Changes

Intel® 845M Chipset Family Specifications Update(s)

NO.	B0/B1	
		There are no specification changes in this Specification Update revision

Errata

Intel® 845MP Chipset (MCH-M) Errata

NO.	B0	PLANS	Intel 845MP® Chipset (MCH-M) ERRATA
1	X	Doc	Possible memory corruption and/or system hang after exit from C3/C4/S1m power states.
2	X	Doc	Noise on DQS pin upon exit of C3/C4/S1m power states may hang the system.

Intel® 845MZ Chipset Errata

NO.	B1	PLANS	Intel® 845MZ Chipset (MCH-M) ERRATA
			There is no errata

Specification Clarifications

NO.	B0/B1	SPECIFICATION CLARIFICATIONS
		There are no specification changes

Documentation Changes

NO.	B0/B1	DOCUMENTATION CHANGES
		There are no documentation changes

Specification Changes

There are no specification changes in this Specification Update.

Errata

Intel® 845MP Chipset Errata

1. Possible memory corruption and/or system hang after exit from C3/C4/S1m power states.

Problem: Upon exit of C3,C4 and S1m power states system memory can become corrupt potentially resulting in system hang.

Implication: It has been determined when MCH-M DLLs are re-enabled upon exit of C3 and S1m power states system memory may become corrupted. The inability to re-enable MCH-M DLLs upon exit of C3 and S1m power states, requires they are enabled throughout C3 and S1m transitions. This will result in reduced power savings in C3 and S1m power states.

Workaround: Current S/W leaves MCH-M DLLs enabled throughout C3 and S1m power state transitions.

Status: Implemented in S/W workaround

2. Noise on DQS pin upon exit of C3/C4/S1m power states may hang the system.

Problem: The 845MP DDR interface can perform false reads when resuming from C3, C4 or S1m power states. This will result in continued offset reads eventually leading to a system hang during resume. The initial false read(s) are a result of noise on the DQS lines propagating through to an internal state machine during a very short period of time early in the resume process.

Implication: If the 845MP internal state machine gets improperly incremented, incorrect memory will get accessed leading to a system hang.

Workaround: BIOS to set MCH-M bit 10 of device 6, offset 78h to prevent noise on DQS from propagating through, during sense amp power up, and causing internal state machine to incorrectly incrementing during resume.

Status: Implemented in S/W workaround

Intel® 845MZ Chipset Errata

1. There is no Errata

Specification Clarifications

There are no specification clarifications in this Specification Update.

Documentation Changes

There are no documentation changes in this Specification Update.